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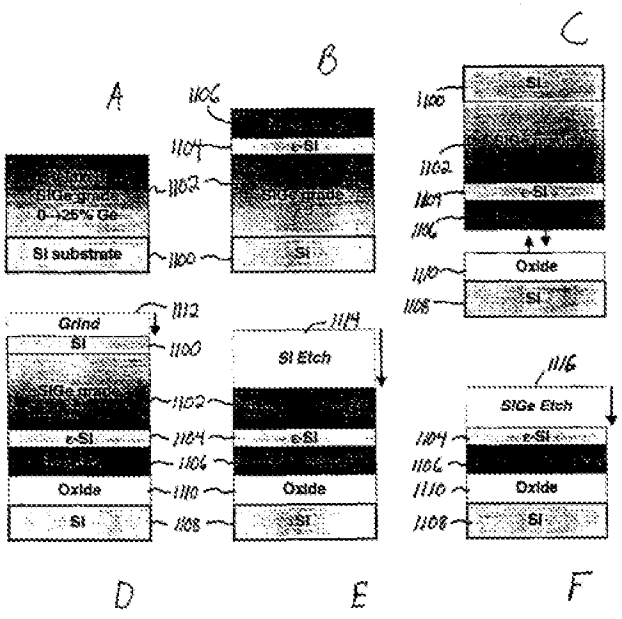
(54) Title: ETCH STOP LAYER SYSTEM



(57) Abstract: A SiGe monocrystalline etch-stop material system on a monocrystalline silicon substrate. The etch-stop material system can vary in exact composition, but is a doped or undoped $Si_{1-x}Ge_x$ alloy with x generally between 0.2 and 0.5. Across its thickness, the etch-stop material itself is uniform in composition. The etch stop is used for micromachining by aqueous anisotropic etchants of silicon such as potassium hydroxide, sodium hydroxide, lithium hydroxide, ethylenediamine/pyrocatechol/pyrazine (EDP), TAM, and hydrazine. These solutions generally etch any silicon containing less than $7x10^{19}$ cm^{-3} of boron or undoped $Si_{1-x}Ge_x$ alloys with x less than approximately 18. Alloying silicon with moderate concentrations of germanium leads to excellent etch selectivities, i.e., differences in etch rate versus pure undoped silicon. This is attributed to the change in energy band structure by the addition of germanium. Furthermore, the nondegenerate doping in the $Si_{1-x}Ge_x$ alloy should not affect the etch-stop behavior. The etch-stop of the invention includes the use of a graded-composition buffer between the silicon substrate and the SiGe etch-stop material. Nominally, the buffer has a linearly-changing composition with respect to thickness, from pure silicon at the substrate/buffer interface to a composition of germanium, and dopant if also present, at the buffer/etch-stop interface which can still be etched at an appreciable rate. Here, there is a strategic jump in germanium and concentration from the buffer side of the interface to the etch-stop material, such that the etch-stop layer is considerably more resistant to the etchant. This process and layer structure allows for an entire range of new materials for microelectronics. The etch-stop capabilities introduce new novel processes and structures such as relaxed SiGe alloys on Si, SiO_2, and SiO_2/Si. Such materials are useful for future strained Si MOSFET devices and circuits.

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ETCH STOP LAYER SYSTEM

BACKGROUND OF THE INVENTION

The invention relates to the field of etch-stop material systems on monocrystalline silicon.

Microelectromechanical systems (MEMS) form the bridge between conventional microelectronics and the physical world. They serve the entire spectrum of possible applications. MEMS include such varied devices as sensors, actuators, chemical reactors, drug delivery systems, turbines, and display technologies. At the heart of any MEMS is a physical structure (a membrane, cantilever beam, bridge, arm, channel, or grating) that is "micromachined" from silicon or some other electronic material. Since MEMS are of about the same size scale and, ideally, fully integrated with associated microelectronics, naturally they should capitalize on the same materials, processes, equipment, and technologies as those of the microelectronics industry. Because the process technology for silicon is already extensively developed for VLSI electronics, silicon is the dominant material for micromachining. Silicon is also mechanically superior to compound semiconductor materials and, by far, no other electronic material has been as thoroughly studied.

A wide array of micromachined silicon devices are fabricated using a high boron concentration "etch-stop" layer in combination with anisotropic wet etchants such as ethylenediamine and pyrocatechol aqueous solution (EDP), potassium hydroxide aqueous solution (KOH), or hydrazine (N_2H_2). Etch selectivity is defined as the preferential etching of one material faster than another and quantified as the ratio of the faster rate to the slower rate. Selectivity is realized for boron levels above 10^{19} cm^{-3}, and improves as boron content increases.

It should be noted that etch stops are also used in bond and etch-back silicon on insulator (BESOI) processing for SOI microelectronics. The etch-stop requirements differ somewhat from those of micromachining, e.g., physical dimensions and defects, but the fundamentals are the same. Hence, learning and development in one area of application can and should be leveraged in the other. In particular, advances in relaxed SiGe alloys as substrates for high speed electronics suggests that a bond-and-etch scheme for creating SiGe-on-insulator would be a desirable process for creating high speed and wireless communications systems.

SUMMARY OF THE INVENTION

Accordingly, the invention provides a SiGe monocrystalline etch-stop material

system on a monocrystalline silicon substrate. The etch-stop material system can vary in exact composition, but is a doped or undoped $Si_{1-x}Ge_x$ alloy with x generally between 0.2 and 0.5. Across its thickness, the etch-stop material itself is uniform in composition. The etch stop is used for micromachining by aqueous anisotropic etchants of silicon such as potassium hydroxide, sodium hydroxide, lithium hydroxide, ethylenediamine/ pyrocatechol/ pyrazine (EDP), TMAH, and hydrazine. For example, a cantilever can be made of this etch-stop material system, then released from its substrate and surrounding material, i.e., "micromachined", by exposure to one of these etchants. These solutions generally etch any silicon containing less than $7x10^{19}$ cm^{-3} of boron or undoped $Si_{1-x}Ge_x$ alloys with x less than approximately 18.

Alloying silicon with moderate concentrations of germanium leads to excellent etch selectivities, i.e., differences in etch rate versus pure undoped silicon. This is attributed to the change in energy band structure by the addition of germanium. Furthermore, the nondegenerate doping in the $Si_{1-x}Ge_x$ alloy should not affect the etch-stop behavior.

The etch-stop of the invention includes the use of a graded-composition buffer between the silicon substrate and the SiGe etch-stop material. Nominally, the buffer has a linearly-changing composition with respect to thickness, from pure silicon at the substrate/ buffer interface to a composition of germanium, and dopant if also present, at the buffer/ etch-stop interface which can still be etched at an appreciable rate. Here, there is a strategic jump in germanium and concentration from the buffer side of the interface to the etch-stop material, such that the etch-stop layer is considerably more resistant to the etchant.

In accordance with the invention there is provided a monocrystalline etch-stop layer system for use on a monocrystalline Si substrate. In one embodiment of the invention, the system includes a substantially relaxed graded layer of $Si_{1-x}Ge_x$, and a uniform etch-stop layer of substantially relaxed $Si_{1-y}Ge_y$. In another embodiment of the invention, the system includes a substantially relaxed graded layer of $Si_{1-x}Ge_x$, a uniform etch-stop layer of substantially relaxed $Si_{1-y}Ge_y$, and a strained $Si_{1-z}Ge_z$ layer. In yet another embodiment of the invention, the system includes a substantially relaxed graded layer of $Si_{1-x}Ge_x$, a uniform etch-stop layer of substantially relaxed $Si_{1-y}Ge_y$, a second etch-stop layer of strained $Si_{1-z}Ge_z$, and a substantially relaxed $Si_{1-w}Ge_w$ layer.

In accordance with the invention there is also provided a method of integrating device or layer. The method includes depositing a substantially relaxed graded layer of $Si_{1-x}Ge_x$ on a Si substrate; depositing a uniform etch-stop layer of substantially relaxed

$Si_{1-y}Ge_y$ on the graded buffer; and etching portions of the substrate and the graded buffer in order to release the etch-stop layer.

In accordance with another embodiment of the invention, there is provided a method of integrating a device or layer. The method includes depositing a substantially relaxed graded layer of $Si_{1-x}Ge_x$ on a Si substrate; depositing a uniform first etch-stop layer of substantially relaxed $Si_{1-y}Ge_y$ on the graded buffer; depositing a second etch-stop layer of strained $Si_{1-z}Ge_z$; depositing a substantially relaxed $Si_{1-w}Ge_w$ layer; etching portions of the substrate and the graded buffer in order to release the first etch-stop layer; and etching portions of the residual graded buffer in order to release the second etch-stop $Si_{1-z}Ge_z$ layer.

BRIEF DESCRIPTION OF THE DRAWINGS

FIGs. 1A-1D are functional block diagrams of exemplary epitaxial SiGe etch stop structures configured on a silicon substrate in accordance with the invention;

FIG. 2 is a cross-sectional TEM micrograph of the structure of FIG. 1B;

FIG. 3 is a cross-sectional TEM micrograph of the structure of FIG. 1C;

FIG. 4 is graph of dopant concentrations of the structure of FIG. 1A;

FIG. 5 is a graph of dopant concentrations of the structure of FIG. 1D;

FIG. 6A is a graph showing the cylindrical etch results of the structure of FIG. 1A; FIG. 6B is graph showing a magnification of the left side of FIG. 6A;

FIG. 7 is a graph showing the cylindrical etch results of the structure of FIG. 1D;

FIG. 8 is a graph showing the etch rates for <100> intrinsic silicon in 34% KOH at 60°C normalized by 18.29 μm/hr of the structures of FIGs. 1A-1D;

FIG. 9 is a photograph of a top view of a micromachined proof mass;

FIG. 10 is a block diagram of a process for fabricating an SiGe-on-insulator structure;

FIG. 11A-11F are schematic diagrams of the fabrication process for SiGeOI;

FIGs. 12A and 12B are IR transmission images of intrinsic voids due to particles at the bonding interface, and a demonstration of void-free bonding, and crack due to Maszara surface energy test for SiGe bonded to oxide prior to annealing, respectively;

FIG. 13 is a graph of oxide thickness versus oxidation time, for 700°C wet oxidation of SiGe alloys for various Ge concentration;

FIG. 14 is a graph showing the etching results using a $HF:H_2O_2:CH_3COOH$ (1:2:3) solution, for the a test structure shown in inset diagram;

FIG. 15 is a cross-sectional TEM micrograph of a final exemplary SiGe on oxide structure; and

FIG. 16 is an atomic force microscope surface map of the remaining strained Si layer in the SiGeOI structure, after the 30 minute $HF:H_2O_2:CH_3COOH$ (1:2:3) etch.

DETAILED DESCRIPTION OF THE INVENTION

In the traditional method of forming etch stops in Si micromachining or in certain SOI processes, good etch-stop results are only obtained at very high concentrations of boron, and the dopant's effect on the silicon crystal structure becomes vitally important. Substitution of a silicon atom site with boron, a smaller atom than silicon, contracts the silicon lattice. As the doped lattice remains coherent with the lattice of the undoped substrate, a biaxial "lattice mismatch" stress is generated in the plane of the substrate. This stress biaxially elongates, i.e., elastically strains, the doped material in the same plane. As the base of a unit cell is strained, so is the height via Poisson distortion. Therefore, the Si:B lattice is vertically contracted as it is horizontally expanded, leading to a smaller vertical lattice constant than the equilibrium value. For thin layers of Si:B, it is energetically favorable for the material to be elastically strained like this, i.e., "pseudomorphic".

As the thickness of the doped layer grows, however, the total strain energy per unit area of film increases proportionally, until the layer surpasses a "critical thickness" when it is energetically favorable to introduce dislocations instead of elastically straining the film. Dislocation loops are heterogeneously nucleated at the film surface or film edges and grow larger, gliding towards the substrate-film interface. When a loop meets the interface, the two ends (now called "threading" dislocations because they traverse the thickness of the film) continue to travel away from each other, trailing a line defect at the interface known as a "misfit" dislocation. The misfit dislocations accommodate the lattice-mismatch stress, relieving the horizontal and vertical strains and restoring the in-plane and perpendicular lattice constants to the equilibrium value, i.e., "relaxing" the material. For a low-mismatched lightly strained epitaxial film on a diamond cubic or zincblende substrate, a mesh of orthogonal <110> misfit dislocations is the most likely configuration because of the {111}<110> easy slip system for these crystal structures at elevated temperatures, such as those involved in diffusion and most CVD processes.

At high enough quantities, the effects of any dissimilar-sized substitutional atom on the silicon microstructure are the same as those of boron. Of course, the impact depends on the relative size and concentration of the substitutional species. Also, incorporation of a larger atom than silicon, e.g., germanium, would result in compressive stress and strain rather than a tensile situation like Si:B.

In the conventional etch stop process, extremely high concentrations of boron are needed to achieve a high etch rate selectivity. These very high boron concentrations lead to dislocation introduction in the thick films that are desired in many MEMS applications. Since the p++ process is created usually through a diffusion process, there is a gradient in dislocation density and a gradient in the boron concentration. Because the etch stops in the boron concentration gradient, the thin film part typically possesses large curvature, which is compensated for by an annealing treatment. In addition, the etch stop selectivity is extremely sensitive to the boron concentration. If the concentration falls below the critical $7x10^{19}cm^{-3}$, the selectivity is drastically different. Thus, since this boron concentration is near the solubility limit, dopant concentration fluctuations in the vertical and lateral dimensions produce low yields in MEMS processes. The SiGe etch stop breaks the link between dopant concentration and etch selectivity. Also, since the SiGe alloy is a miscible alloy system, there is continuous complete solubility between Si and Ge.

The theory of anisotropic etching of silicon as described by Seidel et al., J. Electrochem. Soc. 137 , pp. 3626-31 (1990), incorporated herein by reference, is widely considered the appropriate model. Although specifics like absolute etch rate and dissolution products may differ, the general concept is valid for all anisotropic etchants, as they are all aqueous alkaline solutions and the contribution of the etchant is modeled as nothing more specific than H_2O and OH^-. Indeed, the existing literature shows consistent behavior among the etchants.

Early work on etch rate reduction in p++ Si:B presented no hypotheses beyond empirical data. Two possible explanations for the etch-stop phenomenon were proposed: stronger bonding from the high boron concentration or the formation of a boron-based passivation layer. As research accumulated, the etch-stop theories aligned along two credible approaches. The electronic models assign etch-stop behavior to the action of carriers while the passivation models directly attribute it to the formation of a passivating oxide-based layer on the silicon surface.

Others concluded that the etch-rate decrease is sensitive to hole concentration and not to atomic concentration of boron or stress. They observed an etch rate drop

that was proportional to the fourth power of the increase in boron concentration beyond about $3x10^{19}$ cm^{-3}. Four electrons are required by a red-ox etching process they described, leading them to explain the etch-stop effect in p++ material as an increased probability that the electrons are lost to Auger recombination because of the higher hole concentrations.

Seidel et al. agreed with the electron recombination hypothesis. They saw the etch rate begin to fall around $2\text{-}3x10^{19}$ cm^{-3}, which agrees with the doping level for the onset of degeneracy, $2.2x10^{19}$ cm^{-3}. At degeneracy, the Fermi level drops into the valence band and the band-bending is confined to a thickness on the order of one atomic layer. The injected electrons needed for etching are able to tunnel through such a narrow potential well and recombine in the p++ bulk crystal, which halts the etching reaction. The remnant etch rate in the etch-stop regime is attributed to the conduction band electrons, whose quantity is inversely proportional to the hole, i.e. boron, concentration. Four electrons are required to etch one silicon atom, which explains the dependence of the remnant etch rate on the fourth power of the boron concentration.

It was observed that the formation of an SiO_X passivation layer on p++ Si:B($2x10^{20}cm^{-3}$) in aqueous KOH by *in situ* ellipsometric measurements. In the case of p^+ -Si, a large number of holes at the surface causes spontaneous passivation with a thin oxide-like layer. The layer is not completely networked like thermal oxide, so it is etched faster and there is still transport of reactants and etch products across the layer, leading to some finite overall etch rate. The lattice strain induced by a high dopant concentration could enhance the layer's growth. Furthermore, the etch rate reduction is not a Fermi-level effect since the phenomenon is exhibited by both heavily doped p- and n-silicon.

Chen et al., J. Electrochem. Soc. 142, p.172 (1995), assimilated the observations and hypotheses above and their own findings into a composite electrochemical model, where etch stopping is attributed to the enhancement of the oxide film growth rate under high carrier concentration. The key process is hole-driven oxidation at the interface, which inhibits etching by competing with a reaction for Si-Si bonds and hydroxyl radicals, but more importantly, by building the SiO_X barrier. In p++ silicon, a sufficient quantity of holes for etch-stop behavior is supplied as the converse of the electron action outlined by Seidel et al. That is, instead of electrons thermally escaping the potential well or tunneling through into the bulk crystal, holes from the bulk crystal thermally overcome or tunnel through the potential barrier to the interface. It will be

appreciated that this etch-stop process is dynamic, i.e., it is a continuous competition of silicon dissolution and formation/ dissolution of the oxide-like layer, whose net result is a nonzero etch rate.

Germanium is appealing as an etch-resistant additive because it is isoelectronic to, and perfectly miscible in, silicon and diffuses much less readily than dopants and impurities in silicon. Furthermore, the epitaxy of silicon-germanium alloys is selective with respect to silicon oxide, facilitating patterning and structuring, and even affords higher carrier mobilities to electronics monolithically integrated with MEMS.

Existing germanium-based etch-stop systems are, at best, only marginally suitable for silicon micromachining. In spite of the aforementioned advantages to using germanium, currently there is an inadequate understanding of the etch-stop effect in silicon-germanium materials and no information on anisotropic etching of high germanium content solid solutions.

Many isotropic etchants for pure germanium exist. Common to all of these is an oxidizer, such as HNO_3 or H_2O_2, and a complexing agent to remove the oxide, like HF or H_3PO_4. Early studies were made on isotropic germanium etching by solutions such as "Superoxol", a commercially available H_2O_2-HF recipe. More recently, investigations have been made on various combinations of HNO_3, HNO_2, HF, H_2SO_4, H_2SO_2,CH_3COOH, H_2O_2, and H_2O.

In fact, some of these compositions selectively etch germanium or silicon-germanium alloys over silicon, because of differences in the relative oxidation or oxide dissolution rates, but only one etchant exhibits the inverse preference relevant to this project: 100% NH_4OH at 75°C directly attacks polysilicon at 2.5 μm/hr but polygermanium at only 660 Å/hr. Unfortunately, the selectivity is only about 37, the etch rate for silicon is impracticably slow, and the etch is isotropic, which limits its usefulness in micromachining.

Previous results with heavy concentrations of germanium in silicon are likewise discouraging with respect to silicon micromachining. Shang et al., J. Electrochem. Soc. 141, p. 507 (1994), incorporated herein by reference, obtained a selectivity of 6 for relaxed, dislocated $Si_{0.7}Ge_{0.3}$:B (10^{19} cm^{-3}) in a KOH-propanol-$K_2Cr_2O_7$ aqueous solution. Yi et al., Mat. Res. Soc. Symp. Proc. 3779, p. 91 (1995), developed a novel NH_4NO_3-NH_4OH etchant with selectivities better than 1000 at 70°C for 10% and higher germanium alloys. The mixture does not etch pure germanium, but etches pure silicon at 5.67 μm/hr, a weak pace for micromachining purposes. Both systems are isotropic.

By holding the $Si_{0.7}Ge_{0.3}$:B film under the critical thickness, Shang's team improved the selectivity in the same KOH-propanol-$K_2Cr_2O_7$ solution to about 40. Narozny et al., IEEE IEDM (1988) 563, were the first to use such a "strain-selective" recipe, but only realized a selectivity of 20 (for 30% germanium doped with 10^{18} cm^{-3} boron) and a sluggish etch rate of 1.5 μm/hr at room temperature for pure silicon.[26] Although the results of Shang *et al.* and Narozny et al. might have simply been from the well-established etch-stop ability of boron, Godbey et al., Appl. Phys. Lett. 56, p. 374 (1990), achieved a selectivity of 17 with undoped $Si_{0.7}Ge_{0.3}$. None of the articles on strain-selective etchants offer an explanation for the selectivity.

The anemic etch rate is a grave disadvantage because many MEMS structures can be fairly large compared to typical VLSI dimensions. Moreover, MEMS structures subjected to strain-selective etchants would have to be thinner than the critical thickness. However, as a pseudomorphic structure is released and its strain relieved, the selectivity would deteriorate. A sacrificial strained etch-stop layer could be used, imposing additional process steps and design constraints, but would at least provide advantages over current oxide/ nitride sacrificial layers: monocrystallinity can continue above the layer and silicon-germanium's growth selectivity with respect to oxide adds design/ patterning freedom.

The consensus of the research community has been that low concentrations of germanium have little or no effect on etch stopping in anisotropic etchants like KOH and EDP. Up to 12% germanium, Seidel et al. detected no significant suppression of etch rate. p++ layers strain-compensated with 2% germanium showed no remarkable differences from those without germanium. By implanting germanium, Feijóo et al., J. Electrochem. Soc. 139, pp. 2312-13 (1992), attained a maximum selectivity of 12 to 24 in EDP at 80°C, corresponding to a dose with a peak concentration of about 0.6%.

Finne et al., J. Electrochem. Soc. 114, p.969 (1967), however, observed that $Si_{1-x}Ge_x$ solid solutions with x as small as 0.05 did not etch in an ethylenediamine-pyrocatechol-water (EPW) solution. This discrepancy may be attributed to the use of {111} wafers, where accurate measurements are difficult because etching in the <111> direction is very slow. No other information has been reported on germanium-rich alloys in anisotropic media.

Corresponding to the ostensible ineffectiveness of germanium as an etch-stop agent in most publications, there has been little discussion of the source of the limited selectivity that has been detected. Seidel et al. cautioned that their model for heavily-doped boron etch stops is not applicable to germanium because the element is

isoelectronic to silicon. They assumed instead that the small reduction of the etch rate is either due to changes in the energy band structure, or else a consequence of the extremely high concentration of lattice defects such as misfit dislocations which could act as recombination centers.

The invention provides a SiGe monocrystalline etch-stop material system on a monocrystalline silicon substrate. The etch-stop material system can vary in exact composition, but is a doped or undoped $Si_{1-x}Ge_x$ alloy with x generally between 0.2 and 0.5. Across its thickness, the etch-stop material itself is uniform in composition. The etch stop is used for micromachining by aqueous anisotropic etchants of silicon such as potassium hydroxide, sodium hydroxide, lithium hydroxide, ethylenediamine/ pyrocatechol/ pyrazine (EDP), TMAH, and hydrazine. For example, a cantilever can be made of this etch-stop material system, then released from its substrate and surrounding material, i.e., "micromachined", by exposure to one of these etchants. These solutions generally etch any silicon containing less than $7x10^{19}$ cm^{-3} of boron or undoped $Si_{1-x}Ge_x$ alloys with x less than approximately 18.

Thus, it has been determined that alloying silicon with moderate concentrations of germanium leads to excellent etch selectivities, i.e., differences in etch rate versus pure undoped silicon. This is attributed to the change in energy band structure by the addition of germanium. Furthermore, the nondegenerate doping in the $Si_{1-x}Ge_x$ alloy should not affect the etch-stop behavior.

The etch-stop of the invention includes the use of a graded-composition buffer between the silicon substrate and the SiGe etch-stop material. Nominally, the buffer has a linearly-changing composition with respect to thickness, from pure silicon at the substrate/ buffer interface to a composition of germanium, and dopant if also present, at the buffer/ etch-stop interface which can still be etched at an appreciable rate. Here, there is a strategic jump in germanium and concentration from the buffer side of the interface to the etch-stop material, such that the etch-stop layer is considerably more resistant to the etchant. For example, the buffer could grade up to $Si_{0.85}Ge_{0.15}$, then jump to a uniform etch-stop layer of $Si_{0.7}Ge_{0.3}$. Nominally, the composition gradient in the buffer is 5-10% Ge/micron, and the jump in Ge concentration is 5-15 relative atomic percent Ge. The buffer and etch-stop materials are deposited epitaxially on a standard silicon substrate, such as by chemical vapor deposition (CVD) or molecular beam epitaxy (MBE). Note in the above example that the germanium concentration leads to etch stop behavior, and therefore doping concentrations in the etch stop can be varied independently, without affecting etch selectivity.

With respect to the effect of crystalline defects on the etch-stop behavior, in accordance with the invention using $Si_{1-x}Ge_x$ alloys, the influence of defects is minimal. The use of a graded buffer suppresses the threading dislocation density (TDD) in the top etch-stop layer, which leads to a uniform, nearly defect-free $Si_{1-x}Ge_x$ etch stop.

The significance of the jump in concentration(s) at the end of the graded region is that the part must be well defined and dimensions well controlled. Thus, a high selectivity should exist between the top etch-stop layer and the end of the graded region for abrupt, predictable etch-stop behavior. A smooth compositional transition from buffer to etch-stop layer would lead to curved edges and greater dimensional variability in the micromachined part, whereas compositional jumps would yield clean, sharp edges and precise dimensions in the released structure. However, if the jump is too large, e.g., greater than ~20-25 atomic% Ge, the corresponding change in lattice constant, i.e., the lattice mismatch, would create defects.

The $Si_{1-x}Ge_x$ etch-stop material system, which can be substituted for heavily boron-diffused layers, broadens the spectrum of available etch-stop materials, including undoped (isoelectronic) materials, thus improving the design flexibility for micromachined structures. For example, standard micromachining processes limit the dimensions of silicon sensor structures to a single uniform thickness. Resonant devices for inertial sensing would benefit considerably from more flexible design in which the resonators are thinner than the seismic mass. The invention provides an enabling technology for such a multi-thickness structure. Such a fundamental advantage makes the novel technology widely applicable to the fabrication of MEMS by silicon micromachining.

A tremendously significant application is the ability to integrate mechanical and electronic devices on the same material. Replacement of the heavily boron-doped etch stop, which is incompatible with integrated circuit (IC) requirements, by isoelectronic and/or moderately-doped etch stops of device quality allows concurrent processing of mechanical devices and associated electronics on the same wafer. Germanium is perfectly miscible in silicon and diffuses much less readily than dopants and impurities. Alloying with germanium also affords higher carrier mobilities to the electronic devices.

Furthermore, epitaxy of $Si_{1-x}Ge_x$ alloys is selective with respective to silicon oxide, which facilitates patterning and structuring. In addition, defects do not seem to affect the etch-stop efficacy of these materials.

In developing the germanium-based etch stops of the invention, standard 3" or 4" phosphorous-doped (2-4 Ωcm) or boron-doped (7-10.2 Ωcm) (001) silicon substrates were used. The wafers were cleaned for 10 minutes in a piranha bath (3:1 95% H_2SO_4 in water: 30% H_2O_2 in water) and 10 seconds in 4.4% HF and DI water. The substrates were then left in the load lock (~10^{-8} Torr) of the vertical UHVCVD reactor overnight. On the following day, the substrates were raised to the lip of the reactor chamber for about two hours to drive off any volatiles, organics, and water. Then the wafers were desorbed of whatever oxide remained by raising them into the 850-900°C reactor chamber for several minutes. A silicon buffer layer on the order of 1 μm was deposited with SiH_4 while the reactor was brought to process temperature. Following this preparation procedure each time, the epitaxial structures were grown in the temperature range 750-900°C using SiH_4, GeH_4, 1% B_2H_6 in H_2, and 1% PH_3 in H_2.

KOH and EDP were used in the etching. KOH is a commonly studied etchant, the simplest and easiest to consider, and relatively easy and safe to use. Although details of absolute etch rate differ, various anisotropic silicon etchants have behaved consistently. Seidel et al.'s well-subscribed theory of anisotropic etching is explicitly etchant-nonspecific. Results, discussions, and conclusions regarding anisotropic etching and etch-stopping of silicon are widely considered to be valid for any anisotropic etchant. Cylindrical etching and patterned oxide masks were both used to determine the efficacy of Ge concentration on etch rate.

To test the utility of the relaxed epitaxial SiGe etch stops, epitaxial structures were fabricated: WU_2, WU_3, WU_4, and UHV_17 as shown in FIGs. 1A-1D. FIG. 1A is a functional block diagram of an epitaxial SiGe etch stop structure 100 (WU_2) configured on a silicon substrate 102. The structure includes a plurality of relaxed graded layers 104 that vary from $Si_{0.98}Ge_{0.02}$, $5x10^{20}cm^{-3}$ B at the substrate surface, to the top surface layer of $Si_{0.74}Ge_{0.26}$, $10^{18}cm^{-3}$ P. The thickness of each layer are provided in μm.

FIG. 1B is a functional block diagram of an epitaxial SiGe etch stop structure 110 (WU_3) configured on a silicon substrate 112. The structure includes a plurality of relaxed graded layers 114 that vary from $Si_{0.99}Ge_{0.01}$ at the substrate surface, to the top surface layer of $Si_{0.84}Ge_{0.16}$.

FIG. 1C is a functional block diagram of an epitaxial SiGe etch stop structure 120 (WU_4) configured on a silicon substrate 122. The structure includes a relaxed graded layer 124 of $Si_{0.66}Ge_{0.34}$.

FIG. 1D is a functional block diagram of an epitaxial SiGe etch stop structure

130 (WU_4) configured on a silicon substrate 132. The structure includes a plurality of relaxed graded layers 134 that vary from $Si_{0.97}Ge_{0.03}$, $3x10^{15}cm^{-3}$ B at the substrate surface, to the top surface layer of $Si_{0.66}Ge_{0.34}$, $4x10^{16}cm^{-3}$ B.

The compositional grading is known to considerably relax the superficial epitaxial layer while effectively suppressing the TDD. The slow grading rate and generous thickness of these epistructures assure a well-relaxed top film. Thus, the graded buffer enables etching experiments on relaxed, high quality, high germanium content alloys, an etching regime that has never been accessible before. As discussed heretofore, prior research dealt with pseudomorphic $Si_{1-x}Ge_x$ layers or low concentrations of germanium to minimize dislocations, or heavy germanium alloys saturated with threading dislocations. Hence, the grading technique permits one to use the intrinsic etch-stop properties of $Si_{1-x}Ge_x$ solid solutions.

Based on the approximate volume of a cross-sectional TEM sample, a single threading dislocation in a TEM sample represents a TDD of about 10^8 cm^{-2}. FIG. 2 is a cross-sectional TEM micrograph of structure 110 (WU_3). The top surface is in the upper right direction. The parallel lines (misfit dislocations) define the graded buffer. No threading dislocations can be found, which confirms high crystalline quality. The blurred vertical bands are "bend contours", an artifact of TEM, not threading dislocations.

The absence of threading dislocations in FIG. 2 confirms that structures 110 (WU_2), 120 (WU_3), and 130 (UHV_17), which were processed in virtually identical fashion, contain very few defects. TDDs in such relaxed, graded structures have been shown to be in the range of 10^5-10^6 cm^{-2}. By omitting the graded buffer, structure 120 (WU_4) was intentionally processed to be significantly imperfect, as verified by FIG. 3. FIG. 3 is a cross-sectional TEM micrograph of structure 120 (WU_4). The top surface is to the right. In contrast to FIG. 2, this film is saturated with threading dislocations, which confirms poor crystalline quality. The misfit dislocations in all four of these samples are buried under such a thick overlayer that they cannot possibly affect etching from the top surface.

Dopant concentrations of structures 100 (WU_2) and 130 (UHV_17) are shown in the graphs of FIGs. 4 and 5 respectively. The dopant concentrations were calculated from the mobilities of pure silicon and pure germanium, as indicated. Since structure 130 (UHV_17) contains 30% germanium, the true boron content lies somewhere in between, closer to the pure silicon line. Regardless, it is clear that the boron doping does not approach the levels needed for etch stopping. Structure 130 was doped p-type

to investigate potential interactions or synergies with germanium that were suppressed in structure 100 by intentional background n-doping.

The characteristics of these materials (top layer) that are relevant to etching are summarized in the following table.

sample	avg %Ge (EDX)	doping [cm^{-3}]	defect density (TEM)
WU_2	26	10^{18} P (SIMS)	Low
WU_3	17	None	Low
WU_4	34	None	High
UHV_17	30	$4x10^{16}$ B (SRP)	Low

Structure 100 (WU_2) was used to identify the critical germanium concentration by cylindrically etching and to obtain etch rate values by etching from the top surface.

The cylindrical etch results of structure 100 (WU_2), as shown in the graph of FIG. 6A, confirm the etch-stop behavior of germanium and narrowed the threshold germanium concentration to the range of 16-22%. It was ensured that there were no effects from boron by doping the film n-type. The terraces on the left of the graph, defined by the round dots, represent the layers in the epistructure. The left scale reflects the depth of each layer while the right scale relates the nominal germanium concentration of each layer. The arc is the initial groove surface, and the square dots trace the etched surface.

FIG. 6B is a magnification of the left side of FIG. 6A. It is clear that the etch rate increases dramatically somewhere around 18-20% germanium, suggesting that the critical germanium concentration is in that vicinity.

The cylindrical etch results of structure 130 (UHV_17), as shown in the graph of FIG. 7, show the etch accelerating dramatically around 4.8-5 μm depth. The 5% Ge/μm grading rate reasonably assures that the threshold germanium concentration is near 20% germanium. The profiles of each side of the groove are shown. The lower bar marks where the profile begins to deviate from the initial grooved shape. The depth of this point appears to be 4.8-5.0 μm below the top surface.

The results of the etch rate tests using oxide windows are presented in the following table.

wafer	at% Ge	concentration Ge [cm^{-3}]	etch rate [μm/hr]
WU_2	25.6	$1.28x10^{22}$	0.070
WU_3	16.9	$8.45x10^{21}$	0.234
WU_4	34.0	$1.70x10^{22}$	0.040
UHV_17	30.0	$1.50x10^{22}$	0.133

The etch rate for <100> intrinsic silicon in 34% KOH at 60°C was taken as 18.29 μm/hr from Seidel *et al.* The experimental data for structures 100 (WU_2), 110 (WU_3), 120 (WU_4), and 130 (UHV_17) are shown in the table. Normalized by 18.29 μm/hr, they are plotted in the graph of FIG. 8 along with Seidel et al.'s points.

Some features in FIG. 8 should be emphasized. First, there was appreciably greater variability, both up and down, in the individual etch rates of "good" structure 120 (WU_4) pieces than of the other good samples, hence the error bar. A comparison of all the data supports the belief that the considerable surface roughness of structure 120 (WU_4), from lattice-mismatch stress and the high TDD, is probably to blame. Thus, the graded layer has already proven its efficacy since the graded layer samples did not display this problem.

The shape of the new curve very closely resembles that of EDP-boron curve, adding confidence in the new data as well as implying the existence of a universal etch-stop model. In addition, KOH, a more environmentally friendly etch stop than EDP, appears to be a better etch stop with SiGe alloy than EDP with the conventional p++ etch stop.

Despite the popular sentiment in the literature, it is indisputable that silicon-germanium alloys with sufficient germanium are exceptional etch stops that rival the most heavily boron-doped materials. Three different etching techniques and two etchant systems, KOH and EDP, conclusively show this. The intersection of the steep portion of the KOH-germanium curve with unity relative etch rate, the so-called "critical concentration" as defined by Seidel et al., appears to be $2x10^{21}$ cm^{-3}, i.e., 4%, for germanium. Although this value is about 100 times greater than their "critical concentration" for boron, higher selectivities can theoretically be attained with germanium because there are neither solid solubility nor electrical activity limits.

The substantial selectivities obtained from the well-relaxed, low-defect sample structures 100 (WU_2), 110 (WU_3), and 130 (UHV_17) indicate that strain, induced by defects or dissimilar atomic radii, is not principally responsible for etch-stop behavior.

Defects do not play a central role in etch resistance. The excellent results from WU_2, WU_3, and UHV_17, relaxed materials with low TDDs, controvert the speculation that lattice defects serving as recombination centers cause the etch stop behavior with germanium or isoelectronic additives, respectively. Furthermore, a comparison of the etch rate of structure 120 (WU_4) to the KOH- germanium trendline indicates that even a high TDD does not influence etch stopping dramatically (if at all),

nor in a predictable fashion.

The immediately attractive explanation for germanium's newfound etch-stop potency in silicon is the mechanism outlined by R. Leancu, *Sensors and Actuators,* A 46-47 (1995) 35-37, incorporated herein by reference. For 15-30% germanium, it seems more logical to interpolate from the bulk properties of pure germanium than to postulate only how germanium influences the properties of otherwise pure silicon. That is, one should give the germanium atom just as much credit as the silicon atom, since it is no longer a dopant, but rather an alloying species in the truest sense. Thus, the silicon-germanium alloys in question should show a palpable influence from the etching characteristics of pure germanium, which include a slow rate in KOH.

Keeping this simple chemistry approach in mind, a completely miscible binary system like silicon-germanium would display a linear dependence of etch rate versus alloy composition. Even without etch rate data at high germanium concentrations, including pure germanium, FIG. 8 plainly illustrates that such is not the case. Along the same lines, it is unclear why there would be some critical concentration of germanium for an etch-stop effect if the etch rate is simply a consequence of chemical structure, i.e., the proportion of each element. In fact, a nonlinear plot and a critical concentration imply that the etch rate is a function of energy band structure rather than chemical structure.

On a related note, FIG. 8 shows that the germanium-KOH curve is remarkably similar in shape, but not necessarily slope, to the boron-EDP curve, which ascribes its shape to the electronic etch-stop theory. It is difficult to imagine that the germanium-KOH data would just happen to resemble the boron-EDP data, based on a completely different model that warns of no applicability to germanium. That is, it is highly improbable that the true etch-stop mechanism for germanium is entirely unrelated to the true mechanism for boron when the shapes agree so well.

There are reasons to consider an energy band model to account for the etch-stop behavior in silicon-germanium solid solutions. First, the $Si_{1-X}Ge_X$ data resemble the p++ Si:B data, including the critical concentration and power-law dependence of the remnant etch rate, and the p++ Si:B data is explained well by energy band effects. At these quantities, germanium is known to markedly change the band structure of silicon. Furthermore, two possible mechanisms for the etch stop effect of germanium were defects and energy bands. Defect enhanced recombination can be eliminated due to our graded layer approach. Energy band structure is the only other possibility.

Pure bulk germanium has an energy bandgap, E_g, of 0.66 eV at room temperature, compared to 1.12eV for pure bulk silicon. Hence, the addition of

germanium to silicon reduces the bandgap: unstrained $Si_{0.7}Ge_{0.3}$, the situation for samples WU_2, WU_3, WU_4, and UHV_17, has an energy gap of approximately 1.04 eV. Germanium also has a smaller electron affinity, χ, than silicon, 4.00eV versus 4.05eV. Thus, the incorporation of germanium decreases the electron affinity as well. As germanium is added, the shrinking bandgap and electron affinity reduce the band-bending, the potential well in the conduction band, and the potential barrier in the valence band.

The height of the potential barrier in the valence band, b, is given by:

$$b = (\chi - d) + \tfrac{1}{2}E_g \qquad [1]$$

for a generic intrinsic semiconductor, where d is the distance of the Fermi level from E=0, the reference vacuum level. It is understood that the bandgap of $Si_{1-X}Ge_X$ does not change perfectly linearly with germanium concentration, but it is not known how electron affinity decreases with increasing germanium content. Nevertheless, if the two functions are approximated as linear, then b is also roughly linearly dependent on germanium concentration.

Adding germanium to intrinsic silicon also increases the amount of equilibrium electrons and holes, n_i and p_i, respectively, via the decreasing bandgap:

$$n_i = p_i = (N_c N_v)^{\frac{1}{2}} \exp\left(-\frac{E_g}{2kT}\right) \qquad [2]$$

where N_C and N_V are the effective density of states in the conduction and valence bands, respectively, k is Boltzmann's constant, and T is temperature. To simplify the description, N_C and N_V will be assumed to be constant and equal to the values for pure silicon. Again, if E_g's dependence on germanium concentration is considered linear, then p_i is exponentially related to germanium concentration.

The increased p_i increases the passivation reaction. For the intrinsic situation, it is assumed that the well/barrier is not sharp enough to allow tunneling. This is especially true for $Si_{1-X}Ge_X$, with the shallower barrier. Furthermore, the inversion layer at the surface is n-type. Then the supply of holes to the passivation reaction is h, the amount of holes from the bulk that overcome the potential barrier thermally. Thus, h is a Boltzmann activated process:

$$h = p_i \exp(-b/kT) \qquad [3]$$

Since p_i is exponentially dependent on germanium content while b is linearly related, h is overall exponentially related to germanium concentration. This can easily

be seen by substituting expressions [1] and [2] into [3], yielding:

$$h = (N_c N_v)^{\frac{1}{2}} \exp\left(\frac{-E_g - \chi + d}{kT}\right) \quad [4]$$

where E_g and χ are linearly dependent on germanium content. If a critical hole concentration exists for interrupting the etch process, then a critical germanium concentration will be observed.

The potential barrier in the valence band increases as the Fermi level moves closer to the valence band, but the hole concentration is significantly increased by p-doping. In fact, the two effects exactly offset each other. In the extrinsic case, the equilibrium hole concentration, p, is defined as:

$$p = n_i \exp\left(\frac{\frac{E_g}{2} - E_F}{kT}\right) \quad [5]$$

$E_g/2\text{-}E_F$ is precisely the change in b when the material is doped. Then, when expression [5] is substituted for p_i in equation [3], $E_g/2\text{-}E_F$ exactly cancels the change in b in expression [3]. Thus, with nondegenerate doping, the value of h never changes from:

$$h = n_i \exp\left(-\frac{b_i}{kT}\right) \quad [6]$$

where b_i is the height of the barrier in the intrinsic material. Thus, a great advantage of the SiGe etch stop is that the etch selectivity depends only on Ge concentration.

Test structures of structure 110 (WU_3), completely undoped material, were fabricated and probed. The structure 110 (WU_3) did not provide the 'hardest' etch stop available with SiGe alloys because the germanium concentration (15-17%) was near the concentration when etch stop selectivity starts to decrease. The results were very promising as shown in FIG. 9. FIG. 9 is a photograph of a top view of a micromachined proof mass 900. Even at these low Ge concentrations, etched parts like the proof mass in FIG. 9 are possible. Higher Ge concentrations in the uniform layer (30%) result in extremely hard etch stops, with selectivities approaching 1000:1.

It is apparent from cylindrical and top surface etching with EDP and KOH and actual structures micromachined in EDP that relaxed silicon-germanium alloys with sufficient germanium are exceptional etch stops. Selectivities as high as 1000, corresponding to 34% germanium, have been obtained in KOH for the <100> direction. Neither strain nor defects are responsible for these results. High defect density does not influence the etch rate of $Si_{1-x}Ge_x$ dramatically. A plot of relative etch rate versus

germanium concentration follows the same shape as p++ Si:B data, including a critical concentration and a power-law dependence of the remnant rate. The etch stop behavior in relaxed SiGe alloys is correlated to changes in band structure, which are solely connected to Ge concentration.

The extremely high etch selectivities achieved with the SiGe etch stop material system of the invention have immediate applications in forming semiconductor/oxide structures. One method of forming silicon on insulator is to bond a Si wafer to another Si wafer that is coated with silicon dioxide. If one of the wafers is thinned, then a thin layer of Si on silicon dioxide/Si is created. Such structures are useful in low power electronics and high speed electronics since the Si active layer is isolated from a bulk Si substrate via the silicon dioxide layer.

The main disadvantage of this process is the difficulty in thinning one side of the silicon substrate-silicon dioxide-silicon substrate sandwich. In order to have high reproducibility and high yield, the entire wafer must be thinned uniformly and very accurately. Buried etch stops have been used with little success. Even buried, thin layers of strained SiGe have been used, but as mentioned earlier these etch demonstrate etch selectivities <<100, and therefore are not sufficient.

The relaxed SiGe alloys of the invention are ideally suited for this type of etch stop. By bonding a structure 1000 of a graded SiGe layer 1004 and a uniform composition layer 1006 on a silicon wafer 1002 to a structure 1008 having a silicon wafer 1010 coated with silicon dioxide 1012, the etch-stop of the invention can be used to create a very uniform relaxed SiGe alloy on silicon dioxide, which in turn is on a silicon wafer. This process is shown schematically in FIG. 10.

Once the structures are bonded through, for example, annealing, the silicon substrate 1002 and graded layer 1004 are selectively etched away. The finished structure 1014 is a SiGe-on-insulator substrate. It will be appreciated that the structure 1008 can also be a bulk insulating material, such as glass or a glass ceramic.

An entire new materials system from which to make highly effective etch stops has been developed. The new system offers many advantages over current technologies. Germanium is isoelectronic to and perfectly soluble in silicon, and hardly diffuses in it. The deposition of silicon-germanium is selective with respect to oxide. Defects do not weaken the etch-stop efficacy. The etch-stop material can be completely undoped, and according to the proposed band structure model, nondegenerate doping does not influence the etch-stop behavior. This affords incredible utility and design flexibility, especially to integration with microelectronics.

To this end, germanium would even afford higher carrier mobilities.

In fact, this etch stop system can easily be used to integrate various strained Si electronics on relaxed SiGe on any desired substrate (*eg*, insulating or semiconductor substrates), where one such system is SiGe on insulator (SiGeOI). More details of this procedure are provided in the following description.

The main approaches for the fabrication of semiconductors on insulator are separation-by-implanted-oxygen (SIMOX) and wafer bonding (followed by etch-back or Smart-Cut). SIMOX involves implantation by oxygen followed by a high temperature anneal, and hence is attractive due to its apparent simplicity. This technique has shown some success for low Ge compositions, but for higher Ge fractions, in particular for $Si_{0.5}Ge_{0.5}$, the buried oxide structure was not demonstrated, due to the thermodynamic instability of $Si_{1-x}Ge_xO_2$. Simply stated, Ge is not incorporated into the oxide, due to the volatile nature of GeO_2, and therefore for high Ge fractions, there are insufficient Si atoms to form a stable oxide. On the other hand, the bonding technique, which involves the bonding of a SiGe wafer to an oxidized handle wafer followed by the removal of excess material, can be applied to any Ge fraction, without the problem of an unstable oxide. In addition, the procedure is general, one can create SiGe on any desired substrate, including any insulating wafer.

The process flow for the bond/etch-back SiGeOI fabrication technique is shown schematically in FIGs. 11A-11F. The process is separated into growth: (a) UHVCVD growth of relaxed SiGe graded buffer followed by CMP, (b) re-growth of strained Si (ε-Si) and SiGe bonding layer, and bond/etch-back steps: (c) wafer bonding to insulating substrate, (d) backside grinding, (e) Si etch stopping in the graded layer, (f) SiGe etch stopping on the strained Si.

During the first growth, a relaxed 2.5 μm compositionally graded SiGe buffer 1102, capped with 2 μm of $Si_{0.75}Ge_{0.25}$ was deposited onto a Si substrate 1100 at 900°C using a UHVCVD reactor. The graded buffer minimizes threading dislocations and ensures that misfit are only present in the graded layers and not in the uniform composition cap, but these underlying misfits still generate strain fields which cause the formation of surface cross-hatch during growth. To eliminate this surface roughness, which would hinder wafer bonding, the wafer was polished (using chemical-mechanical polishing, CMP) until the cross-hatch was no longer visible using Nomarsky microscopy.

Next a strained Si structure 1104, consisting of 12 nm of strained Si, followed by a layer 1106 of 150 nm of $Si_{0.75}Ge_{0.25}$, was grown at 650°C via UHVCVD onto the

polished SiGe wafers. The low growth temperature ensures minimal surface exchange and inter-diffusion, and hence guarantees a sharp interface between the Si and SiGe layers. The strained Si layer acts as an etch stop during the final etch step, and depending on the thickness requirement and surface roughness constraint for the strained Si channel, may possibly also be used as a MOSFET device channel.

The SiGe wafer was then bonded to a thermally oxidized Si wafer 1108, with an oxide layer 1110 thickness of 200 nm. To ensure adequate bonding, a hydrophobic pre-bonding clean was performed on the wafers. The standard RCA clean cannot be employed for this purpose since the SC1 bath etches Ge and hence roughens the SiGe surface. Instead, a piranha clean (10 minutes) followed by a 50:1 HF dip (30 seconds) was used, which leaves the surface hydrophobic. Such a clean was found to lead to stronger bonding than hydrophilic cleans, after subsequent annealing at moderate temperatures. In addition, the wafers must also be bonded in an ultra-clean environment to ensure no intrinsic voids (as shown in the IR image in FIG. 12A) due to particles at the wafer interfaces.

The wafer pair was annealed for 2 hours at 800°C in a nitrogen ambient. The moderate temperature ensures strong bonding, but is low enough to minimize the diffusion of Ge into the strained Si layer. In addition, the 2 hour anneal at this temperature allows the intrinsic hydrogen voids formed during initial annealing to diffuse. The resulting pair was found to be void free using infrared imaging, and the fracture surface energy deduced with the Maszara razor test technique (FIG. 13B) was 3.7 J/m^2 (which is similar to the surface fracture energy found for Si to oxide bonding), demonstrating that the bonding is indeed strong enough to undergo further material processing, without the risk of delamination.

After bonding the wafers, the pair was coated with nitride to protect the backside of the handle wafer during etching. The backside of the SiGe wafer was then ground as at 1112, removing approximately 450 μm, and a first etch as at 1114 was performed on the wafers to remove the remaining Si from the SiGe wafers. Any etch which attacks Si and not SiGe can be used (*eg*, KOH, TMAH). For example, a KOH mixture (30% KOH by weight in water) at 80°C, with an etching time of 2 hours can be employed to remove the backside Si from the SiGe wafer. KOH etches do not significantly attack relaxed $Si_{1-x}Ge_x$ with Ge compositions of roughly 20% or higher, and hence stop near the top of the grade in our buffers. Note here that unlike pure Si, or strained SiGe based structures, the relaxed SiGe layer provides a natural etch stop, thus alleviating the need for a p^{++} stop layer. This flexibility of doping as an independent variable with respect to etch-stop capability is important in designing

device layers for different applications. For example, p^{++} layers are not desired in RF applications.

The next etch 1116 was employed to remove the remaining SiGe, and stop on the strained Si layer 1104. The active ingredient of this etch consists of any Ge oxidizing agent (*eg*, H_2O_2, HNO_3, low temperature wet oxidation), combined with an oxide stripping agent (*eg*, HF). For example, a low temperature (650°C–750 °C) wet oxidation has been found to oxidize SiGe at much faster rates than Si, as shown in FIG. 13; for a 1 hour oxidation at 700°C, $Si_{0.75}Ge_{0.25}$ oxidizes at a rate of 2.5 nm/min, whereas Si has an oxidation rate of roughly 100 times smaller. In combination with a subsequent HF dip, the above oxidation can be used to remove very thin layers of SiGe, while stopping on Si.

A chemical alternative to the above, is a solution of $HF:H_2O_2:CH_3COOH$ (1:2:3), with an etch time of approximately 30 minutes (in the case when the Si etch stops near the 20% Ge region). This has been shown to etch SiGe preferentially, with a very high selectivity; in particular, for relaxed $Si_{0.75}Ge_{0.25}$ versus Si, the selectivity is roughly 300. For demonstration purposes, a test sample consisting of 400 nm relaxed $Si_{0.75}Ge_{0.25}$ on 12 nm strained Si was partially masked and the etch depth versus time was measured using a profilometer. The results in FIG. 14 clearly show the high selectivity, in addition to the relatively fast etch rate of the $Si_{0.75}Ge_{0.25}$ surface layer. An important observation is that the solution was found to etch dislocation threads on the strained Si stop layer preferentially, causing pitting, which in turn lead to breeches in the strained Si layer when the etch time was prolonged.

FIG. 15 shows a TEM cross-sectional image of the SiGeOI structure fabricated using the proposed technique. No structural defects, such as threading dislocations, were observed in the cross-sectional TEM of the SiGe layer. A low density of threads in the 10^5 cm^{-2} range was confirmed via EPD (etch pit density) of both the as-grown and bonded SiGe, which proves that there is no substantial increase in threading dislocations due to the proposed process. This is in contrast to SIMOX, which can possibly introduce many additional defects depending on the material system being implanted. In particular, the threading dislocation for implanted SiGe of various Ge fractions has not yet been reported in the literature.

An AFM scan of the strained Si surface after the final etching, is shown in FIG. 16. The rms roughness was found to be roughly 1.0 nm, with a maximum peak-to-valley difference of 6.4 nm. This demonstrates that although the $HF:H_2O_2:CH_3COOH$ (1:2:3) SiGe etch, has a good selectivity, it leaves the strained Si layer moderately

rough. Hence, when using this etch, the Si etch stop layer might not be smooth enough to double as a device channel, since the surface roughness may affect device performance. If this is so, the easiest and most general approach simply requires the removal of the Si etch stop layer with KOH, or any another Si etch that is selective to the Ge composition being used. The desired device structure can then be grown onto the SiGeOI substrate, including a strained Si surface channel or any other more elaborate structure.

An alternative approach, especially in the case of buried channel devices, would involve the incorporation of the device channel layers into the bonding structure. Either avenue is easily attainable using our flexible bonding/etch-back process. Using this general approach, the benefits of an insulating substrate (or for that matter, any substrate) can easily be applied to any SiGe device, without any constraints on SiGe thickness, Ge composition or insulating layer thickness or type.

Although the present invention has been shown and described with respect to several preferred embodiments thereof, various changes, omissions and additions to the form and detail thereof, may be made therein, without departing from the spirit and scope of the invention.

What is claimed is:

CLAIMS

1. A monocrystalline etch-stop layer system for use on a monocrystalline Si substrate, said system comprising a substantially relaxed graded layer of $Si_{1-x}Ge_x$, and a uniform etch-stop layer of substantially relaxed $Si_{1-y}Ge_y$.

2. The system of claim 1, wherein $x<0.20$.

3. The system of claim 1, wherein $y>0.19$.

4. The system of claim 1, wherein $x<0.20$ and $y>0.19$.

5. The system of claim 1, wherein said $Si_{1-y}Ge_y$ layer is bonded to a second substrate.

6. The system of claim 5, wherein said second substrate comprises Si.

7. The system of claim 5, wherein said second substrate comprises glass.

8. The system of claim 5, wherein said second substrate comprises quartz.

9. The system of claim 5, wherein said second substrate comprises a layer of SiO_2 on a second Si substrate.

10. The system of claim 5, wherein the first Si substrate and graded layer are substantially removed.

11. The system of claim 6, wherein the first Si substrate and graded layer are substantially removed.

12. The system of claim 7, wherein the first Si substrate and graded layer are substantially removed.

13. The system of claim 8, wherein the first Si substrate and graded layer are substantially removed.

14. The system of claim 9, wherein the first Si substrate and graded layer are substantially removed.

15. The system of claim 1, wherein a SiO_2 layer is deposited onto said $Si_{1-y}Ge_y$ layer.

16. The system of claim 15, wherein said SiO_2 layer is bonded to a second substrate.

17. The system of claim 16, wherein said second substrate comprises a layer of SiO_2 on a second Si substrate.

18. The system of claim 16, wherein said second substrate comprises a layer of SiO_2 on a glass substrate.

19. The system of claim 16, wherein said second substrate comprises a layer of SiO_2 on a quartz substrate.

20. The system of claim 16, wherein the first Si substrate and graded layer are substantially removed.

21. The system of claim 17, wherein the first Si substrate and graded layer are substantially removed.

22. The system of claim 18, wherein the first Si substrate and graded layer are substantially removed.

23. The system of claim 19, wherein the first Si substrate and graded layer are substantially removed.

24. The system of claim 10, wherein the surface is planarized.

25. The system of claim 11, wherein the surface is planarized.

26. The system of claim 12, wherein the surface is planarized.

27. The system of claim 13, wherein the surface is planarized.

28. The system of claim 14, wherein the surface is planarized.

29. The system of claim 20, wherein the surface is planarized.

30. The system of claim 21, wherein the surface is planarized.

31. The system of claim 22, wherein the surface is planarized.

32. The system of claim 23, wherein the surface is planarized.

33. A monocrystalline etch-stop layer system for use on a monocrystalline Si substrate, said system comprising a substantially relaxed graded layer of $Si_{1-x}Ge_x$; a uniform etch-stop layer of substantially relaxed $Si_{1-y}Ge_y$; and a strained $Si_{1-z}Ge_z$ layer.

34. The system of claim 33, wherein $z<y$.

35. The system of claim 33, wherein $y>0.18$.

36. The system of claim 33, wherein $y>0.18$ and $z<y$.

37. The system of claim 33, wherein $y>0.18$ and $z=0$.

38. The system of claim 33, wherein said $Si_{1-z}Ge_z$ is bonded to a second substrate.

39. The system of claim 38, wherein said second substrate comprises Si.

40. The system of claim 38, wherein said second substrate comprises glass.

41. The system of claim 38, wherein said second substrate comprises quartz.

42. The system of claim 38, wherein said second substrate comprises a layer of SiO_2 on a second Si substrate.

43. The system of claim 38, wherein the first Si substrate and graded layer are substantially removed.

44. The system of claim 39, wherein the first Si substrate and graded layer are substantially removed.

45. The system of claim 40, wherein the first Si substrate and graded layer are substantially removed.

46. The system of claim 41, wherein the first Si substrate and graded layer are substantially removed.

47. The system of claim 42, wherein the first Si substrate and graded layer are substantially removed.

48. The structure in claim 33 in which a SiO_2 layer is deposited onto said $Si_{1-z}Ge_z$ layer.

49. The system of claim 48, wherein said SiO_2 layer is bonded to a second substrate.

50. The system of claim 49, wherein the second substrate comprises a layer of SiO_2 on a second Si substrate.

51. The system of claim 49, wherein the second substrate comprises a layer of SiO_2 on a glass substrate.

52. The system of claim 49, wherein the second substrate comprises a layer of SiO_2 on a quartz substrate.

53. The system of claim 49, wherein the first Si substrate and graded layer are substantially removed.

54. The system of claim 50, wherein the first Si substrate and graded layer are substantially removed.

55. The system of claim 51, wherein the first Si substrate and graded layer are substantially removed.

56. The system of claim 52, wherein the first Si substrate and graded layer are substantially removed.

57. A monocrystalline etch-stop layer system for use on a monocrystalline Si substrate, comprising a substantially relaxed graded layer of $Si_{1-x}Ge_x$; a uniform etch-stop layer of substantially relaxed $Si_{1-y}Ge_y$; a second etch-stop layer of strained $Si_{1-z}Ge_z$; and a substantially relaxed $Si_{1-w}Ge_w$ layer.

58. The system of claim 57, wherein $y-0.05<w<y+0.05$.

59. The system of claim 57, wherein w=y.

60. The system of claim 57, wherein said $Si_{1-w}Ge_w$ is bonded to a second substrate.

61. The system of claim 60, wherein said second substrate comprises Si.

62. The system of claim 60, wherein said second substrate comprises glass.

63. The system of claim 60, wherein said second substrate comprises quartz.

64. The system of claim 60, wherein said second substrate comprises a layer of SiO_2 on a second Si substrate.

65. The system of claim 60, wherein the first Si substrate and graded layer are substantially removed.

66. The system of claim 61, wherein the first Si substrate and graded layer are substantially removed.

67. The system of claim 62, wherein the first Si substrate and graded layer are substantially removed.

68. The system of claim 63, wherein the first Si substrate and graded layer are substantially removed.

69. The system of claim 64, wherein the first Si substrate and graded layer are substantially removed.

70. The system of claim 57, wherein a SiO_2 layer is deposited onto said $Si_{1-w}Ge_w$ layer.

71. The system of claim 70, wherein said SiO_2 layer is bonded to a second substrate.

72. The system of claim 70, wherein the second substrate comprises a layer of SiO_2 on a second Si substrate.

73. The system of claim 70, wherein the second substrate comprises a layer of SiO_2 on a glass substrate.

74. The system of claim 70, wherein the second substrate comprises a layer of SiO_2 on a quartz substrate.

75. The system of claim 70, wherein the first Si substrate and graded layer are substantially removed.

76. The system of claim 71, wherein the first Si substrate and graded layer are substantially removed.

77. The system of claim 72, wherein the first Si substrate and graded layer are substantially removed.

78. The system of claim 73, wherein the first Si substrate and graded layer are substantially removed.

79. The system of claim 74, wherein the first Si substrate and graded layer are substantially removed.

80. A method of integrating a device or layer comprising:

depositing a substantially relaxed graded layer of $Si_{1-x}Ge_x$ on a Si substrate;

depositing a uniform etch-stop layer of substantially relaxed $Si_{1-y}Ge_y$ on said graded buffer; and

etching portions of said substrate and said graded buffer in order to release said etch-stop layer.

81. The method of claim 80, wherein $x<0.20$.

82. The method of claim 80, wherein $y>0.19$.

83. The method of claim 80, wherein $x<0.20$ and $y>0.19$.

84. The method of claim 80, wherein the etchant used to release the etch-stop layer is KOH.

85. The method of claim 80, wherein the etchant used to release the etch-stop layer is TMAH.

86. The method of claim 80, wherein the etchant used to release the etch-stop layer is EDP.

87. The method of claim 80, wherein the etch-stop is released and the etch-stop layer is planarized.

88. The method of claim 87, wherein the method of planarization is chemical-mechanical polishing (CMP).

89. A method of integrating a device or layer comprising:

depositing a substantially relaxed graded layer of $Si_{1-x}Ge_x$ on a Si substrate;

depositing a uniform first etch-stop layer of substantially relaxed $Si_{1-y}Ge_y$ on said graded buffer;

depositing a second etch-stop layer of strained $Si_{1-z}Ge_z$;

depositing a substantially relaxed $Si_{1-w}Ge_w$ layer;

etching portions of said substrate and said graded buffer in order to release said first etch-stop layer; and

etching portions of said residual graded buffer in order to release the second etch-stop $Si_{1-z}Ge_z$ layer.

90. The method of claim 89, wherein the etchant used to release the second etch-stop layer comprises an oxidant and an oxide stripping agent.

91. The method of claim 90, wherein the oxidant oxidizes Ge much more rapidly than Si.

92. The method of claim 90, wherein the oxidant comprises H_2O_2.

93. The method of claim 90, wherein the stripping agent comprises HF.

94. The method of claim 90, wherein the oxidant comprises H_2O_2 and the stripping agent comprises HF.

95. The method of claim 94, wherein the diluting agent comprises CH_3COOH.

96. The method of claim 95, wherein the ratio of chemicals in the etchant are (1:2:3) for (HF: H_2O_2: CH_3COOH).

97. The method of claim 89, wherein wet oxidation is used to selectively oxidize the $Si_{1-x}Ge_x$ and $Si_{1-y}Ge_y$, thereby acting as an etch-stop with respect to $Si_{1-z}Ge_z$.

98. The method of claim 97, wherein the wet oxidation temperature is <750 degrees Celsius.

99. The method of claim 97, wherein the oxidized layers are removed by an HF and water solution.

100. The method of claim 98, wherein the oxidized layers are removed by an HF solution.

101. The method of claim 90, wherein the $Si_{1-z}Ge_z$ layer is subsequently removed using a selective etchant with respect to the $Si_{1-w}Ge_w$ layer.

102. The method of claim 91, wherein the $Si_{1-z}Ge_z$ layer is subsequently removed using a selective etchant with respect to the $Si_{1-w}Ge_w$ layer.

103. The method of claim 92, wherein the $Si_{1-z}Ge_z$ layer is subsequently removed using a selective etchant with respect to the $Si_{1-w}Ge_w$ layer.

104. The method of claim 93, wherein the $Si_{1-z}Ge_z$ layer is subsequently removed using a selective etchant with respect to the $Si_{1-w}Ge_w$ layer.

105. The method of claim 94, wherein the $Si_{1-z}Ge_z$ layer is subsequently removed using a selective etchant with respect to the $Si_{1-w}Ge_w$ layer.

106. The method of claim 95, wherein the $Si_{1-z}Ge_z$ layer is subsequently removed using a selective etchant with respect to the $Si_{1-w}Ge_w$ layer.

107. The method of claim 96, wherein the $Si_{1-z}Ge_z$ layer is subsequently removed using a selective etchant with respect to the $Si_{1-w}Ge_w$ layer.

108. The method of claim 97, wherein the $Si_{1-z}Ge_z$ layer is subsequently removed using a selective etchant with respect to the $Si_{1-w}Ge_w$ layer.

109. The method of claim 98, wherein the $Si_{1-z}Ge_z$ layer is subsequently removed using a selective etchant with respect to the $Si_{1-w}Ge_w$ layer.

110. The method of claim 99, wherein the $Si_{1-z}Ge_z$ layer is subsequently

removed using a selective etchant with respect to the $Si_{1-w}Ge_w$ layer.

111. The method of claim 100, wherein the $Si_{1-z}Ge_z$ layer is subsequently removed using a selective etchant with respect to the $Si_{1-w}Ge_w$ layer.

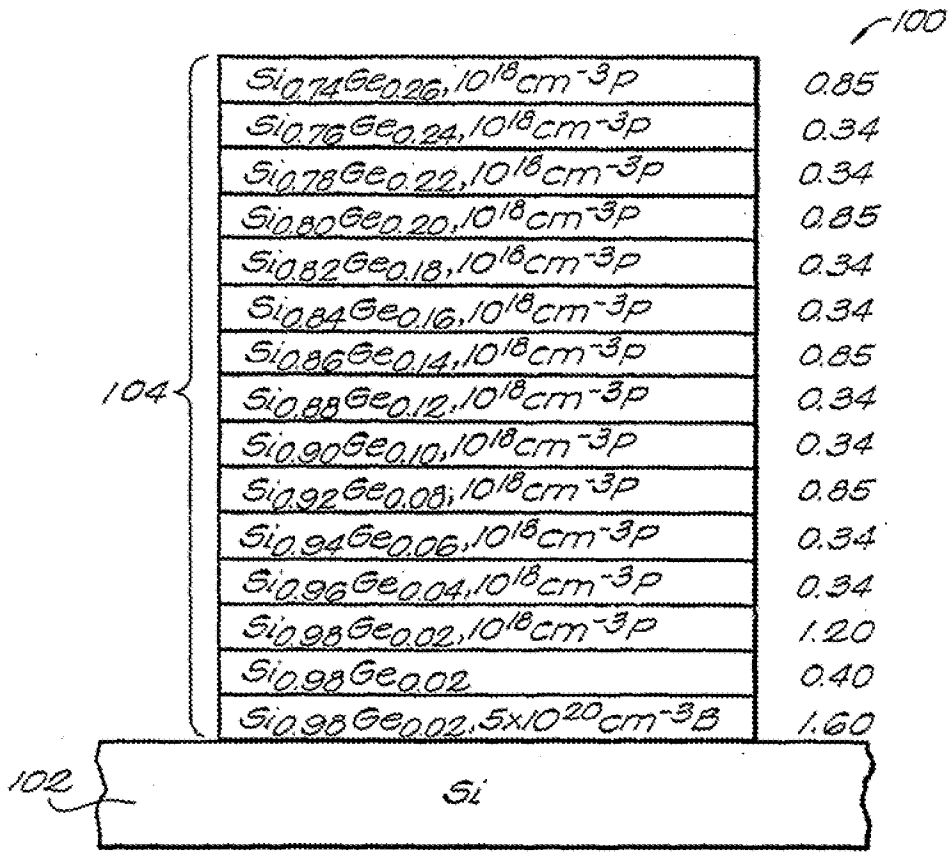

100
$Si_{0.74}Ge_{0.26}, 10^{18}cm^{-3}P$ 0.85
$Si_{0.76}Ge_{0.24}, 10^{18}cm^{-3}P$ 0.34
$Si_{0.78}Ge_{0.22}, 10^{18}cm^{-3}P$ 0.34
$Si_{0.80}Ge_{0.20}, 10^{18}cm^{-3}P$ 0.85
$Si_{0.82}Ge_{0.18}, 10^{18}cm^{-3}P$ 0.34
$Si_{0.84}Ge_{0.16}, 10^{18}cm^{-3}P$ 0.34
$Si_{0.86}Ge_{0.14}, 10^{18}cm^{-3}P$ 0.85
$Si_{0.88}Ge_{0.12}, 10^{18}cm^{-3}P$ 0.34
$Si_{0.90}Ge_{0.10}, 10^{18}cm^{-3}P$ 0.34
$Si_{0.92}Ge_{0.08}, 10^{18}cm^{-3}P$ 0.85
$Si_{0.94}Ge_{0.06}, 10^{18}cm^{-3}P$ 0.34
$Si_{0.96}Ge_{0.04}, 10^{18}cm^{-3}P$ 0.34
$Si_{0.98}Ge_{0.02}, 10^{18}cm^{-3}P$ 1.20
$Si_{0.98}Ge_{0.02}$ 0.40
$Si_{0.98}Ge_{0.02}, 5x10^{20}cm^{-3}B$ 1.60
104
102
Si

FIG. 1A

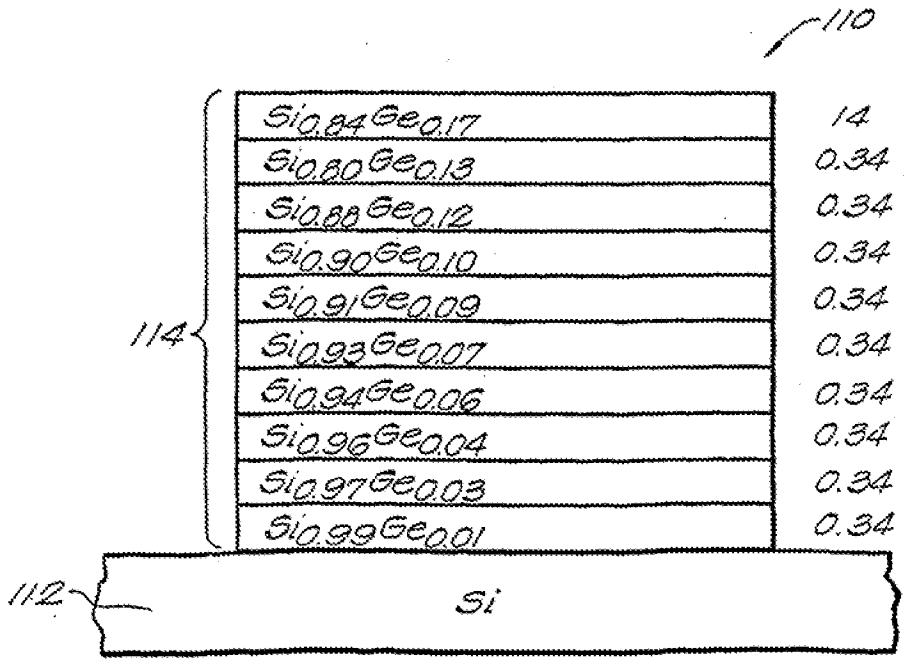

110
$Si_{0.84}Ge_{0.17}$ 14
$Si_{0.80}Ge_{0.13}$ 0.34
$Si_{0.88}Ge_{0.12}$ 0.34
$Si_{0.90}Ge_{0.10}$ 0.34
$Si_{0.91}Ge_{0.09}$ 0.34
$Si_{0.93}Ge_{0.07}$ 0.34
$Si_{0.94}Ge_{0.06}$ 0.34
$Si_{0.96}Ge_{0.04}$ 0.34
$Si_{0.97}Ge_{0.03}$ 0.34
$Si_{0.99}Ge_{0.01}$ 0.34
114
112
Si

FIG. 1B

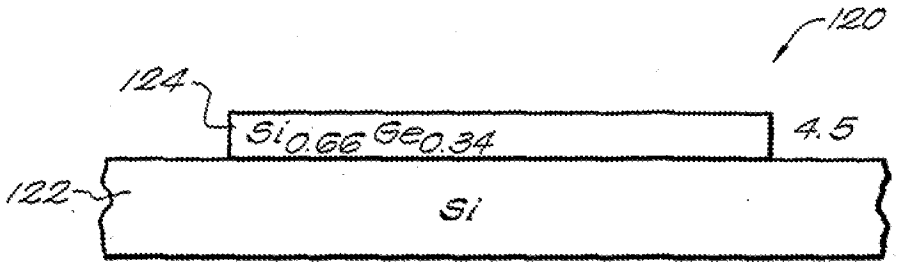

120
124
$Si_{0.66}Ge_{0.34}$
4.5
122
Si

FIG. 1C

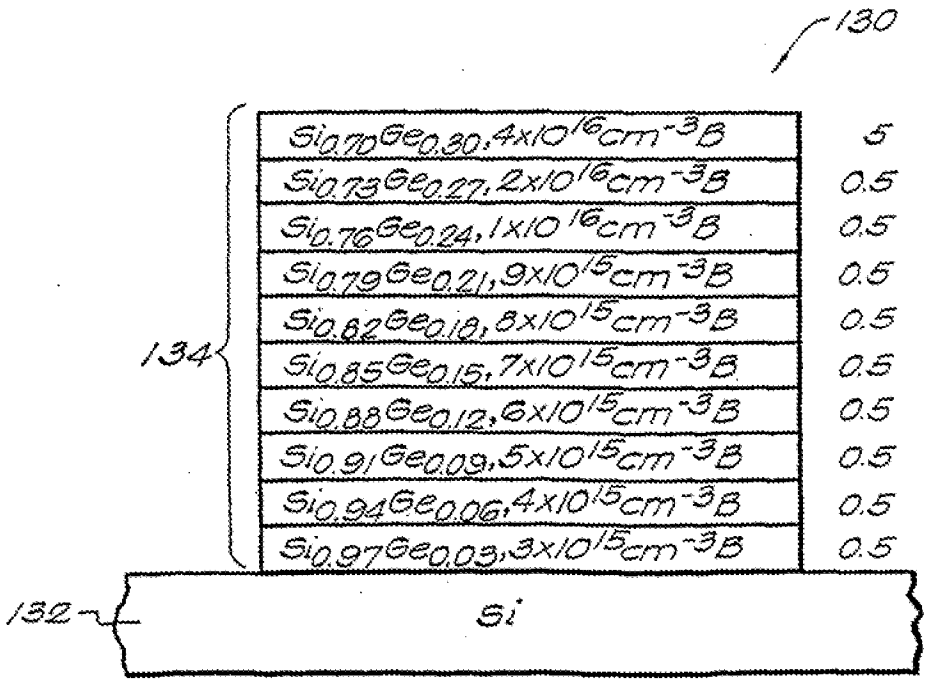

130
$Si_{0.70}Ge_{0.30}, 4x10^{16}cm^{-3}B$ 5
$Si_{0.73}Ge_{0.27}, 2x10^{16}cm^{-3}B$ 0.5
$Si_{0.76}Ge_{0.24}, 1x10^{16}cm^{-3}B$ 0.5
$Si_{0.79}Ge_{0.21}, 9x10^{15}cm^{-3}B$ 0.5
$Si_{0.82}Ge_{0.18}, 8x10^{15}cm^{-3}B$ 0.5
$Si_{0.85}Ge_{0.15}, 7x10^{15}cm^{-3}B$ 0.5
$Si_{0.88}Ge_{0.12}, 6x10^{15}cm^{-3}B$ 0.5
$Si_{0.91}Ge_{0.09}, 5x10^{15}cm^{-3}B$ 0.5
$Si_{0.94}Ge_{0.06}, 4x10^{15}cm^{-3}B$ 0.5
$Si_{0.97}Ge_{0.03}, 3x10^{15}cm^{-3}B$ 0.5
134
132
Si

FIG. 1D

FIG. 2

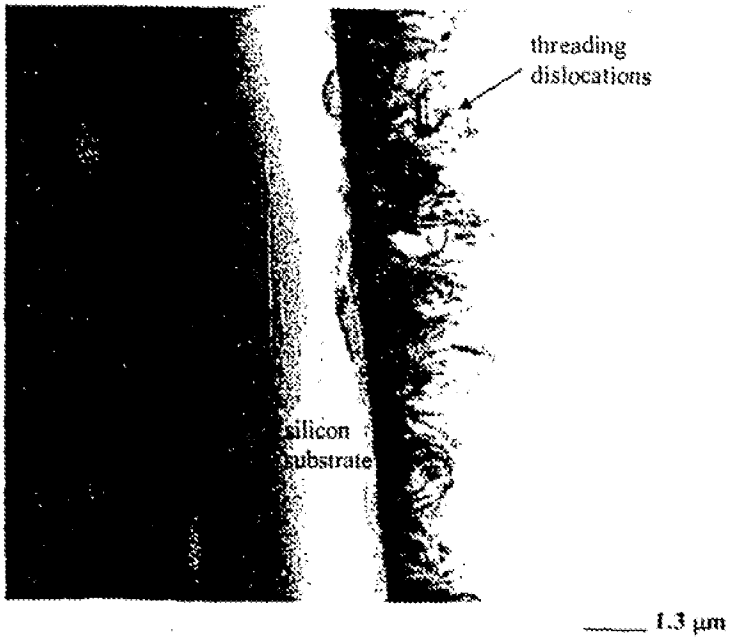


FIG. 3

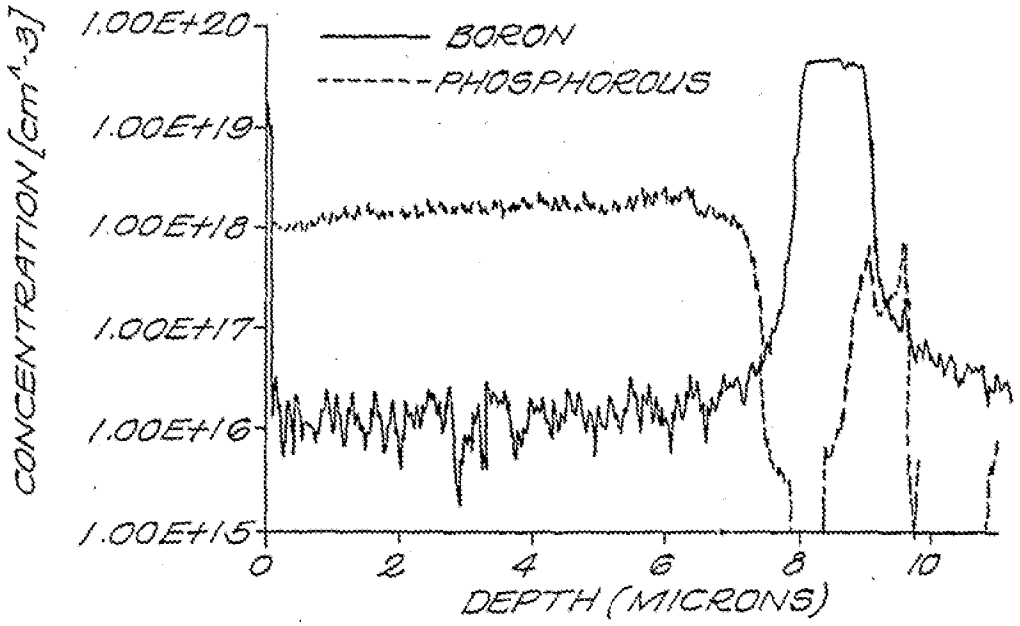

CONCENTRATION [cm^-3]
1.00E+20
1.00E+19
1.00E+18
1.00E+17
1.00E+16
1.00E+15
BORON
PHOSPHOROUS
0
2
4
6
8
10
DEPTH (MICRONS)

FIG. 4

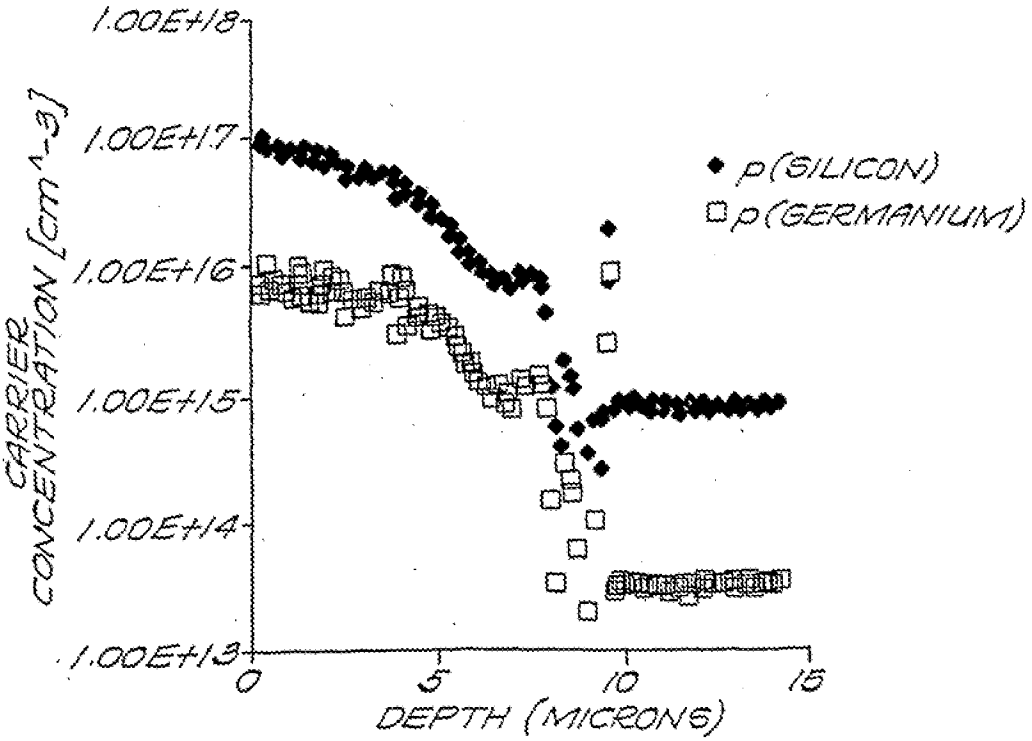

CARRIER CONCENTRATION [cm^-3]
1.00E+18
1.00E+17
1.00E+16
1.00E+15
1.00E+14
1.00E+13
p(SILICON)
p(GERMANIUM)
0
5
10
15
DEPTH (MICRONS)

FIG. 5

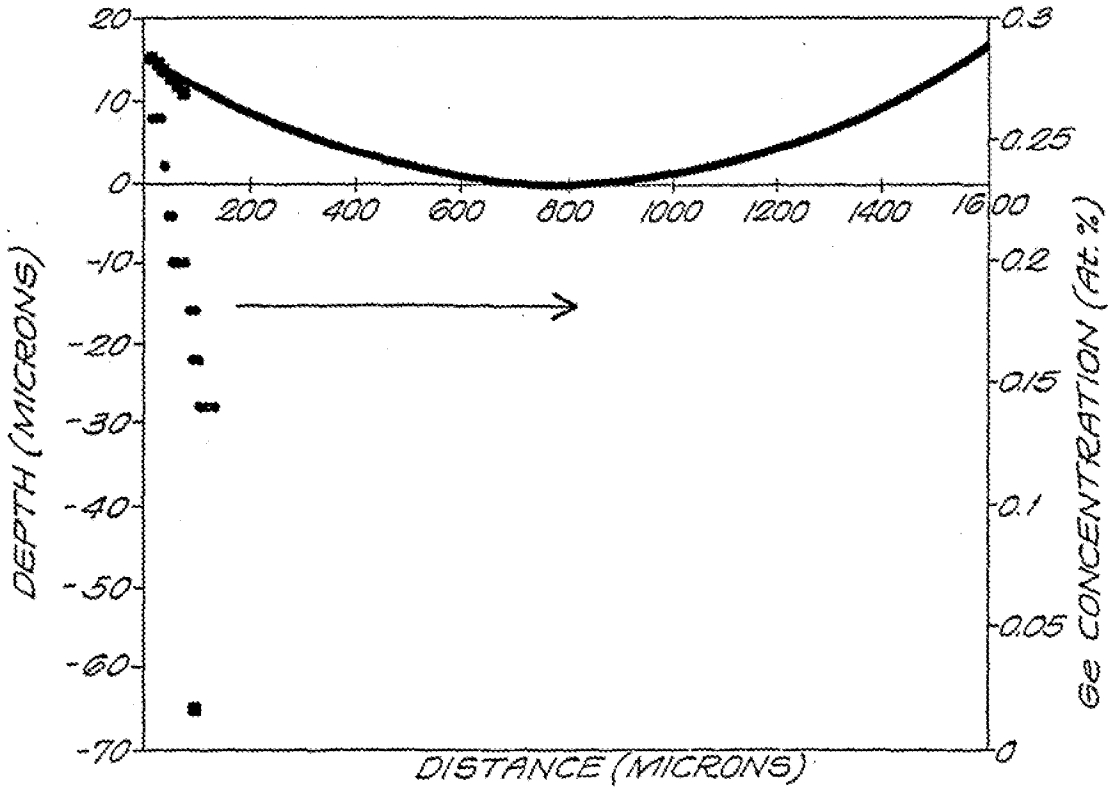

20
10
0
-10
-20
-30
-40
-50
-60
-70
200
400
600
800
1000
1200
1400
1600
0.3
0.25
0.2
0.15
0.1
0.05
0
DEPTH (MICRONS)
DISTANCE (MICRONS)
Ge CONCENTRATION (At.%)

FIG. 6A

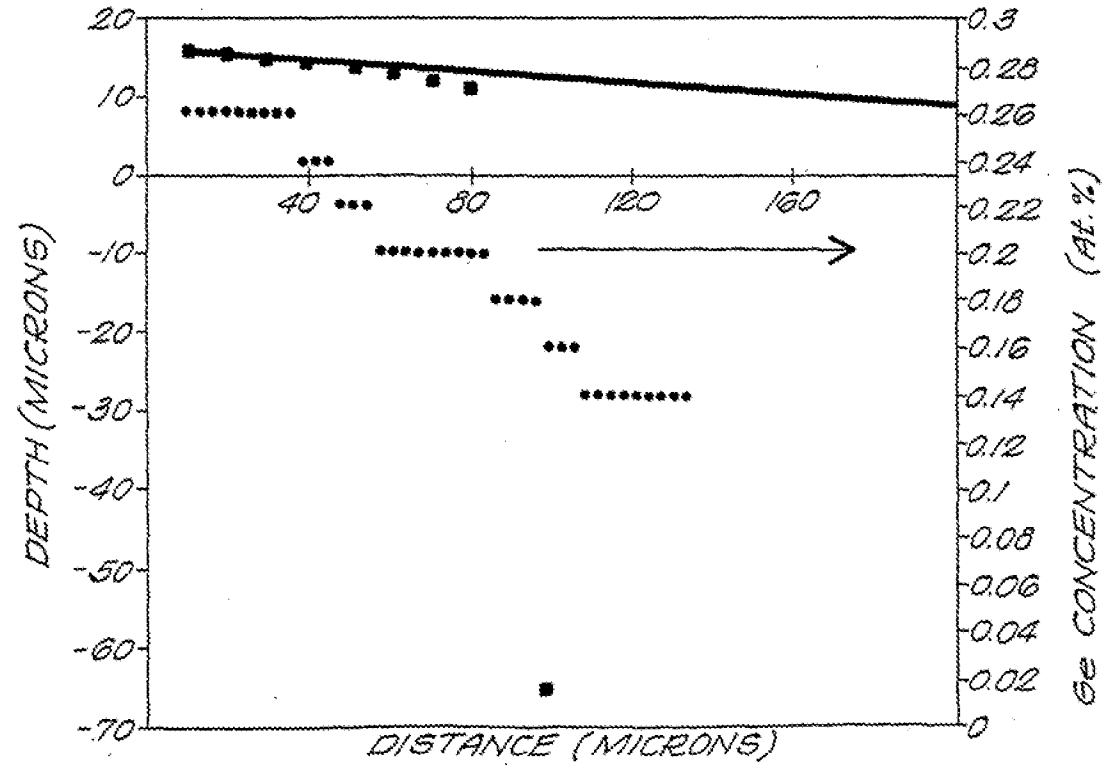

20
10
0
-10
-20
-30
-40
-50
-60
-70
40
80
120
160
0.3
0.28
0.26
0.24
0.22
0.2
0.18
0.16
0.14
0.12
0.1
0.08
0.06
0.04
0.02
0
DEPTH (MICRONS)
DISTANCE (MICRONS)
Ge CONCENTRATION (At.%)

FIG. 6B

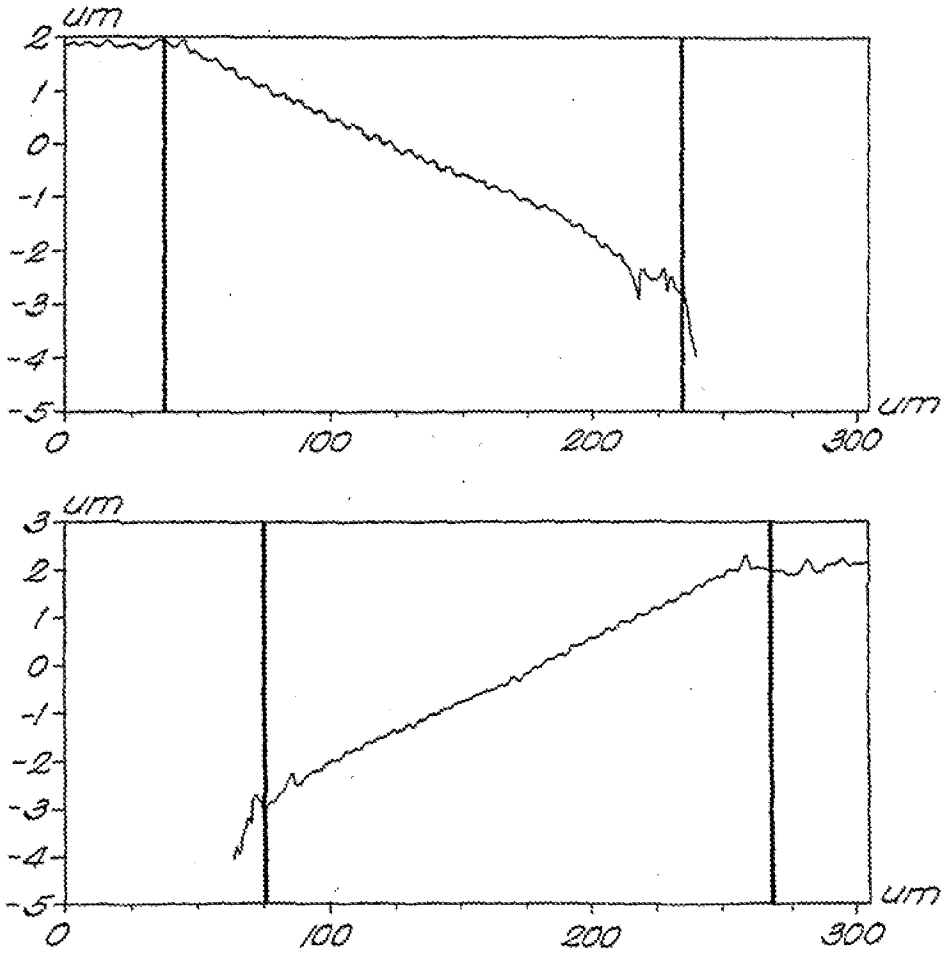


FIG. 7

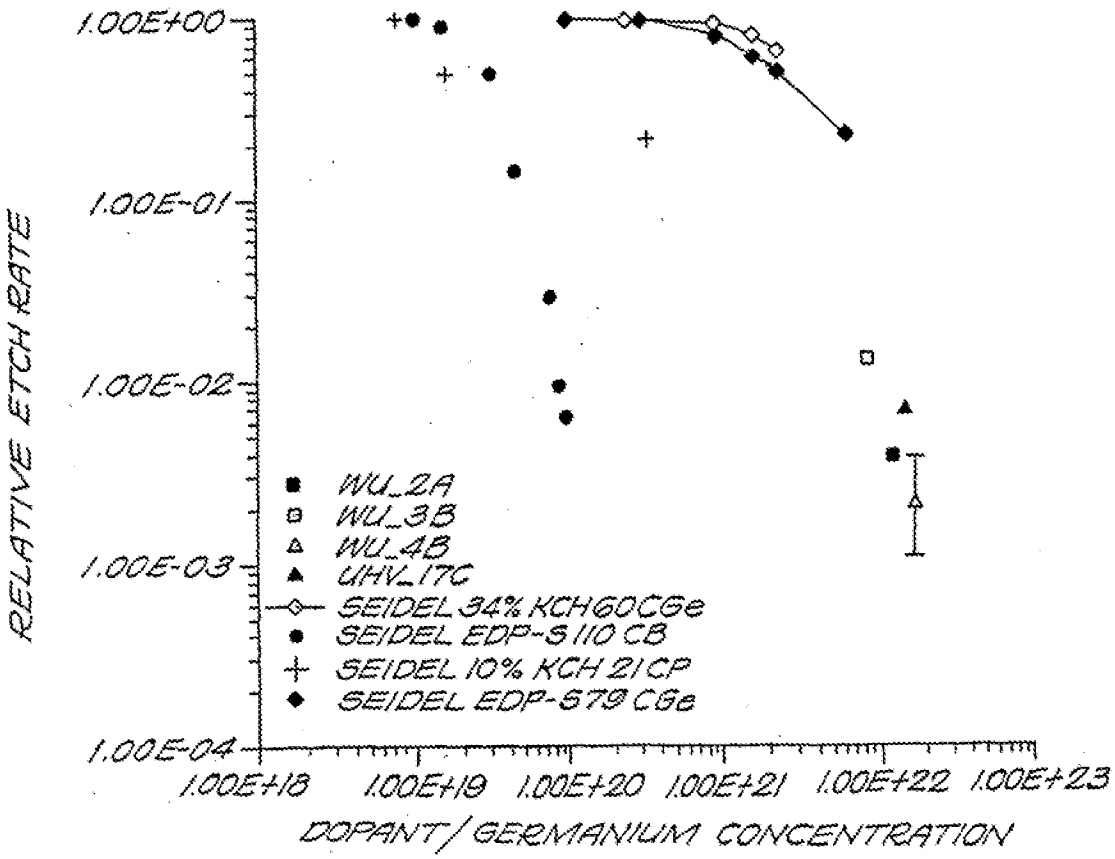

1.00E+00
1.00E-01
1.00E-02
1.00E-03
1.00E-04
RELATIVE ETCH RATE
1.00E+18
1.00E+19
1.00E+20
1.00E+21
1.00E+22
1.00E+23
DOPANT/GERMANIUM CONCENTRATION
WU_2A
WU_3B
WU_4B
UHV_17C
SEIDEL 34% KCH60CGe
SEIDEL EDP-S110 CB
SEIDEL 10% KCH 21CP
SEIDEL EDP-S79 CGe

FIG. 8

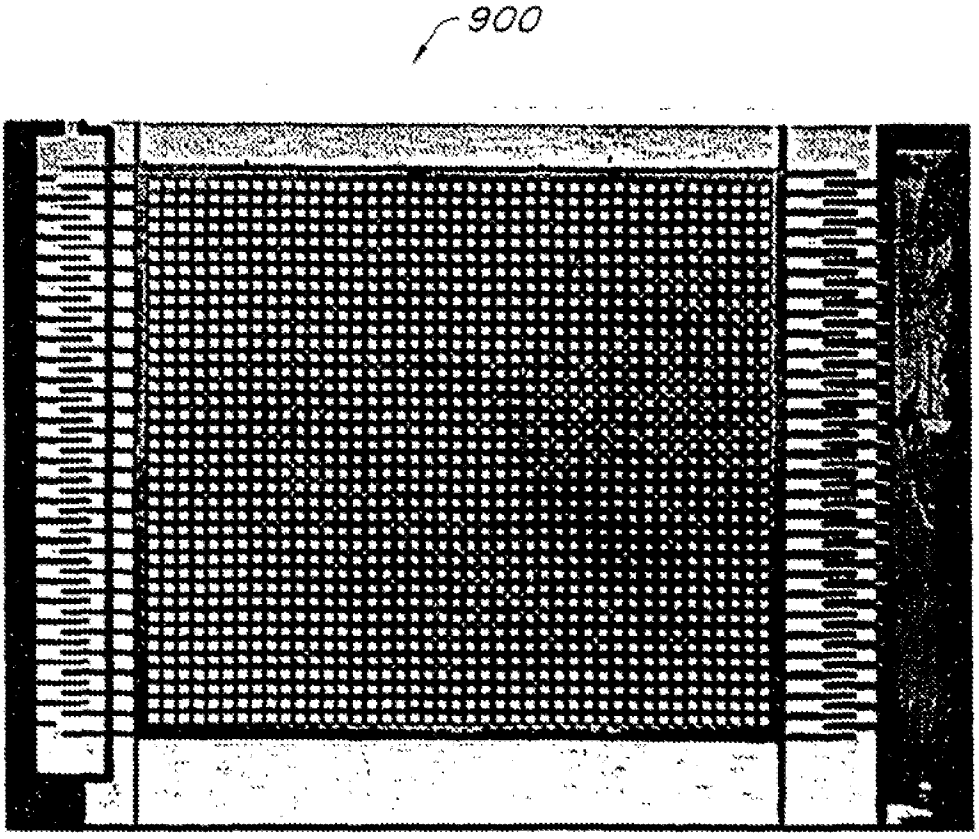


FIG. 9

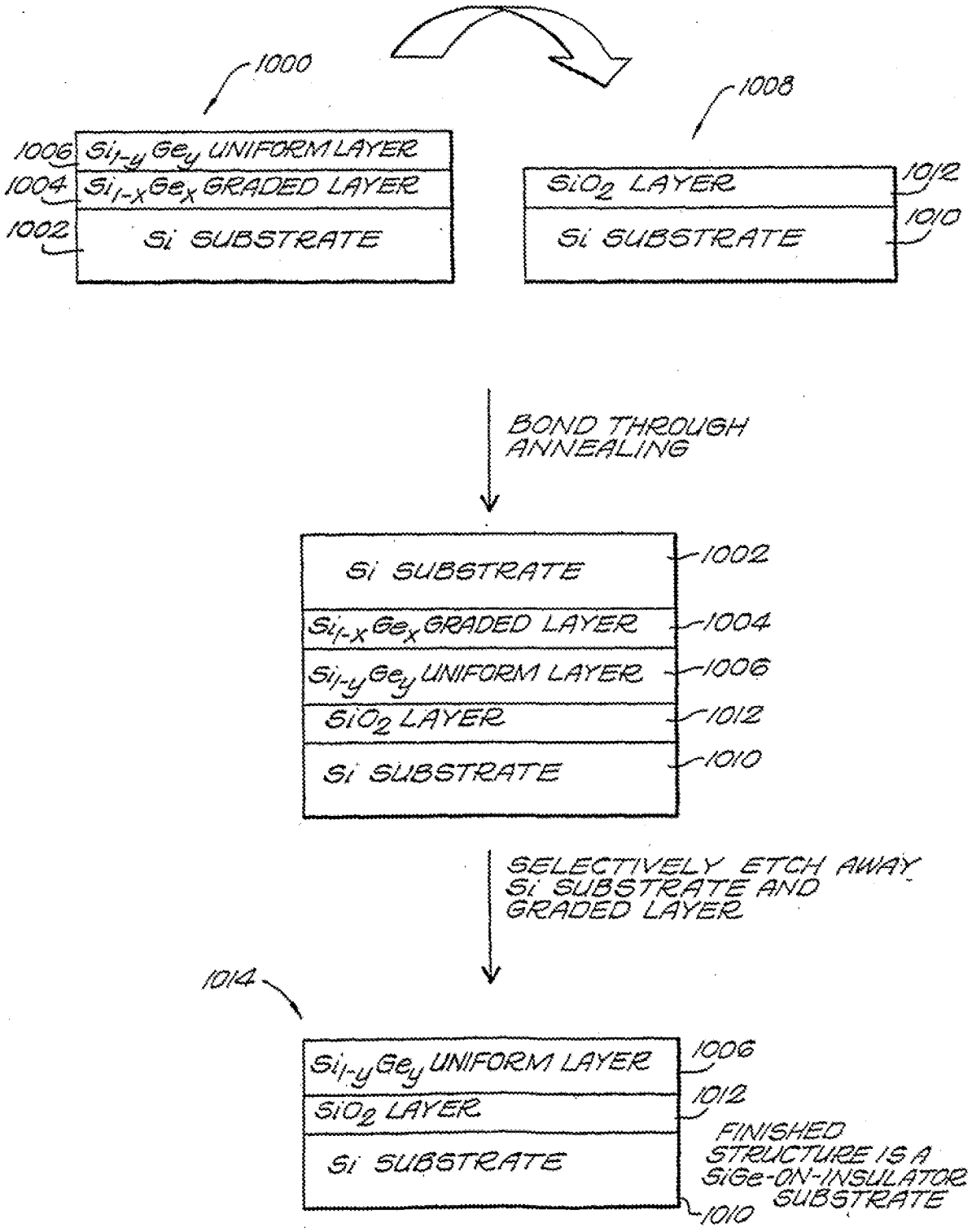

1000
1006
$Si_{1-y}Ge_y$ UNIFORM LAYER
1004
$Si_{1-x}Ge_x$ GRADED LAYER
1002
Si SUBSTRATE
1008
SiO_2 LAYER
1012
Si SUBSTRATE
1010
BOND THROUGH ANNEALING
Si SUBSTRATE
1002
$Si_{1-x}Ge_x$ GRADED LAYER
1004
$Si_{1-y}Ge_y$ UNIFORM LAYER
1006
SiO_2 LAYER
1012
Si SUBSTRATE
1010
SELECTIVELY ETCH AWAY Si SUBSTRATE AND GRADED LAYER
1014
$Si_{1-y}Ge_y$ UNIFORM LAYER
1006
SiO_2 LAYER
1012
Si SUBSTRATE
1010
FINISHED STRUCTURE IS A SiGe-ON-INSULATOR SUBSTRATE

FIG. 10

FIG. 11A

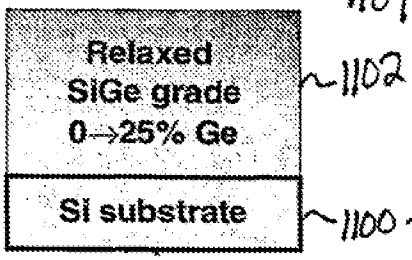


FIG. 11B

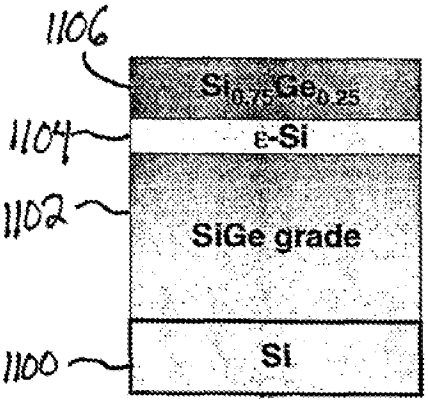
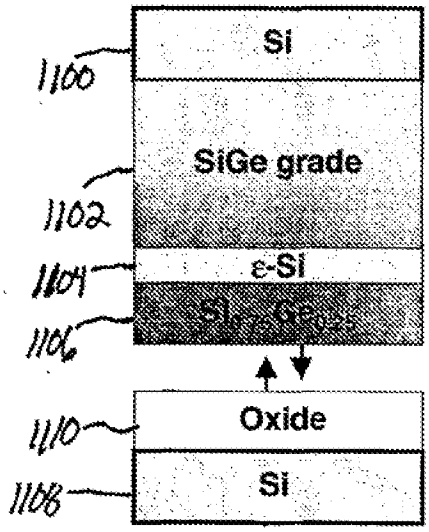


FIG. 11C



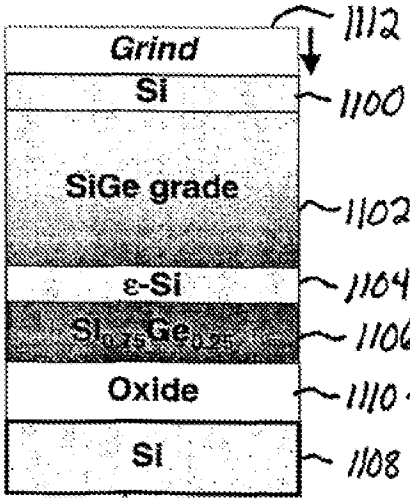


FIG. 11D

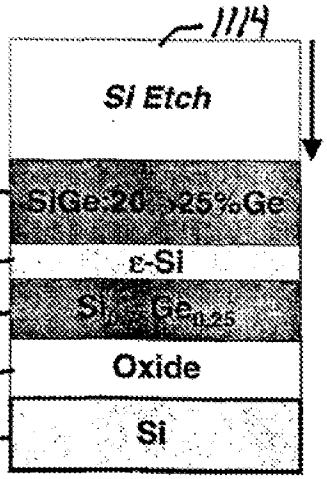


FIG. 11E

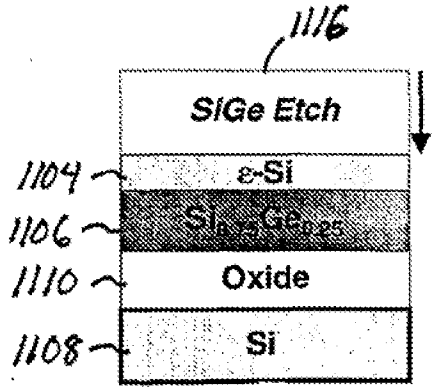


FIG. 11F

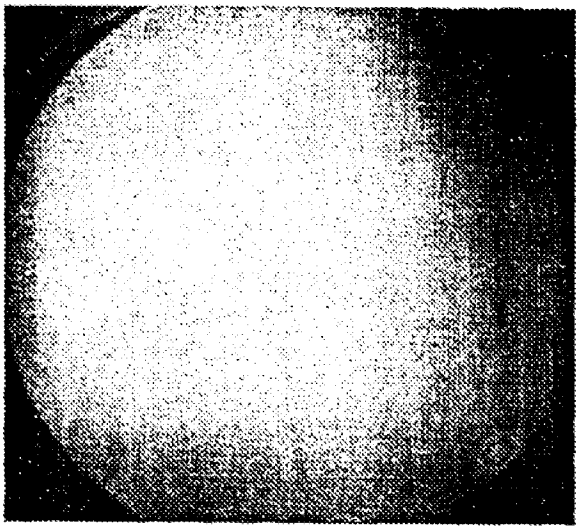


FIG. 12A

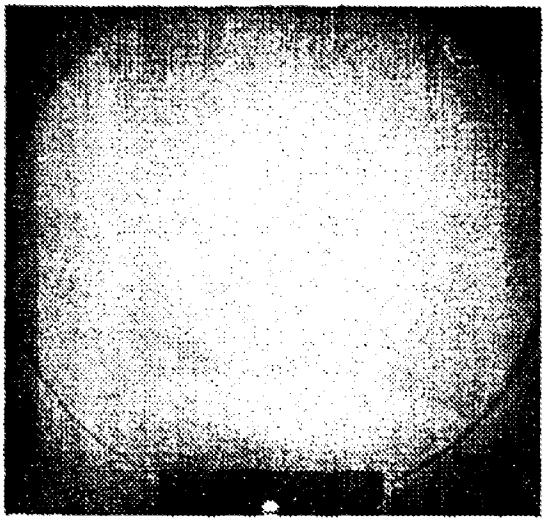


FIG. 12B

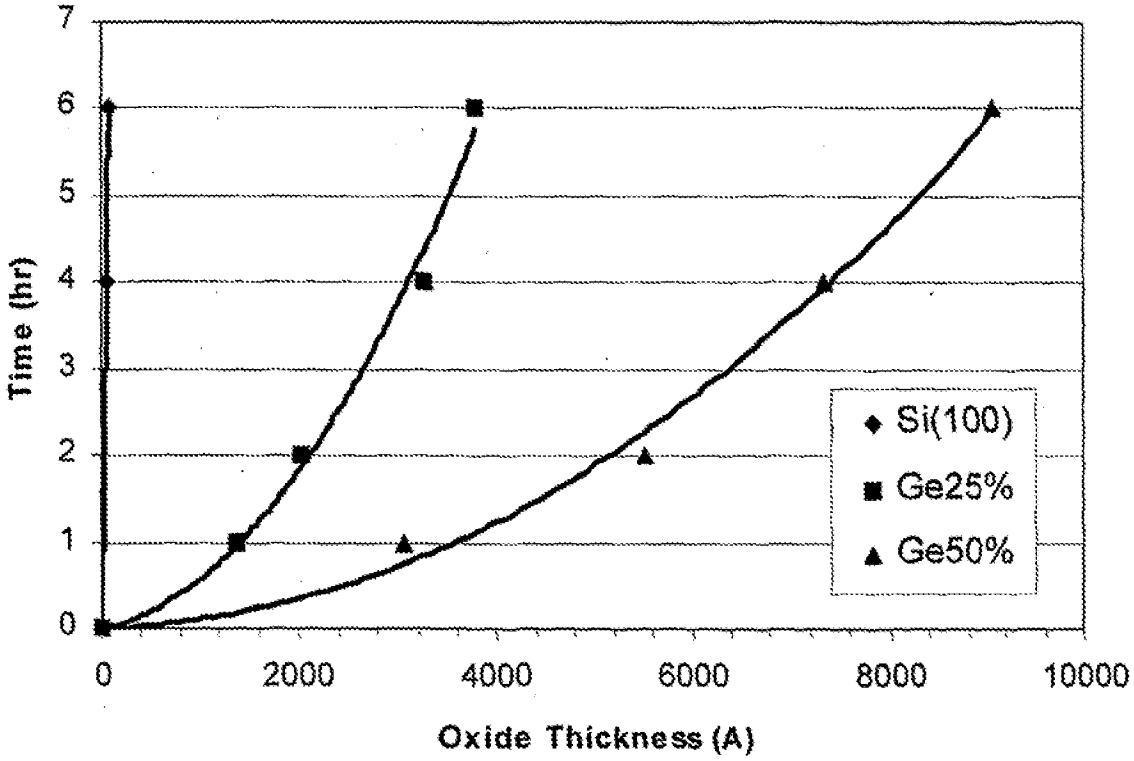

7
6
5
4
3
2
1
0
Time (hr)
0
2000
4000
6000
8000
10000
Oxide Thickness (A)
Si(100)
Ge25%
Ge50%

FIG. 13

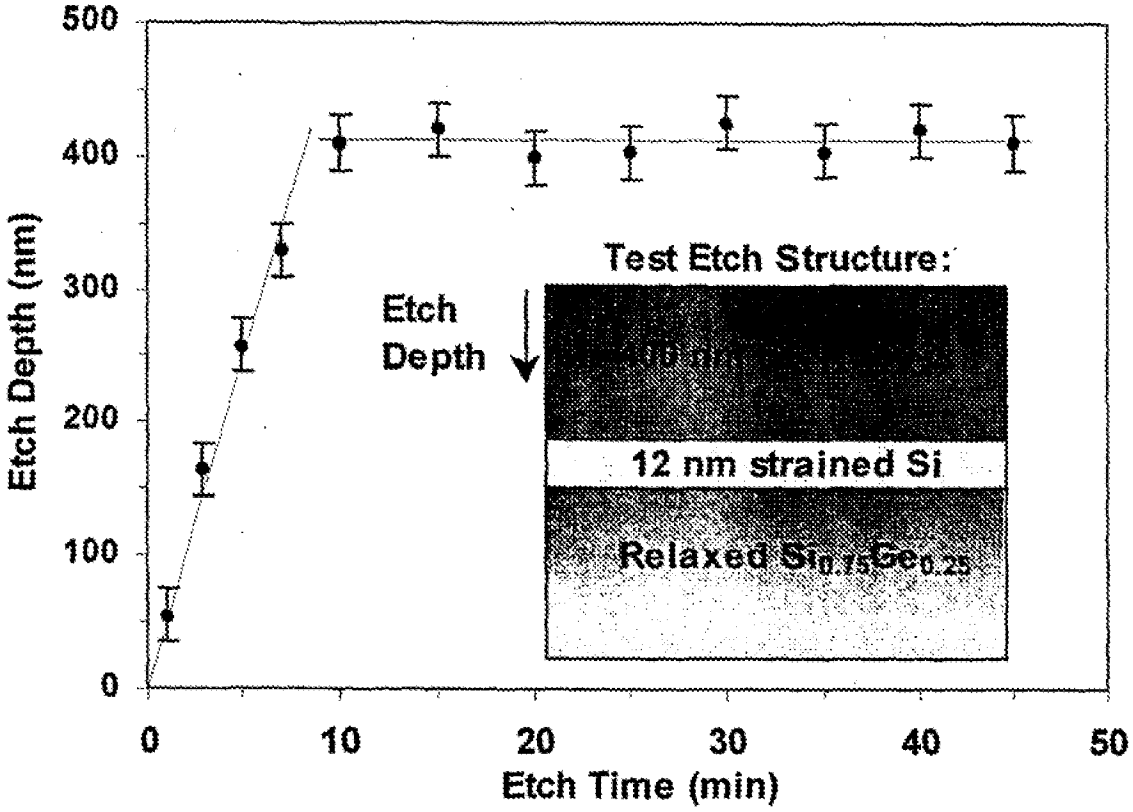

500
400
300
200
100
0
Etch Depth (nm)
0
10
20
30
40
50
Etch Time (min)
Test Etch Structure:
Etch
Depth
400 nm
12 nm strained Si
Relaxed Si0.75Ge0.25

FIG. 14

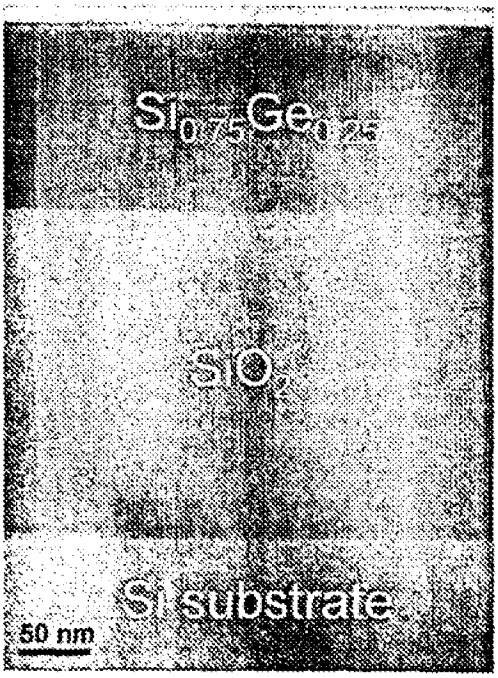


FIG. 15

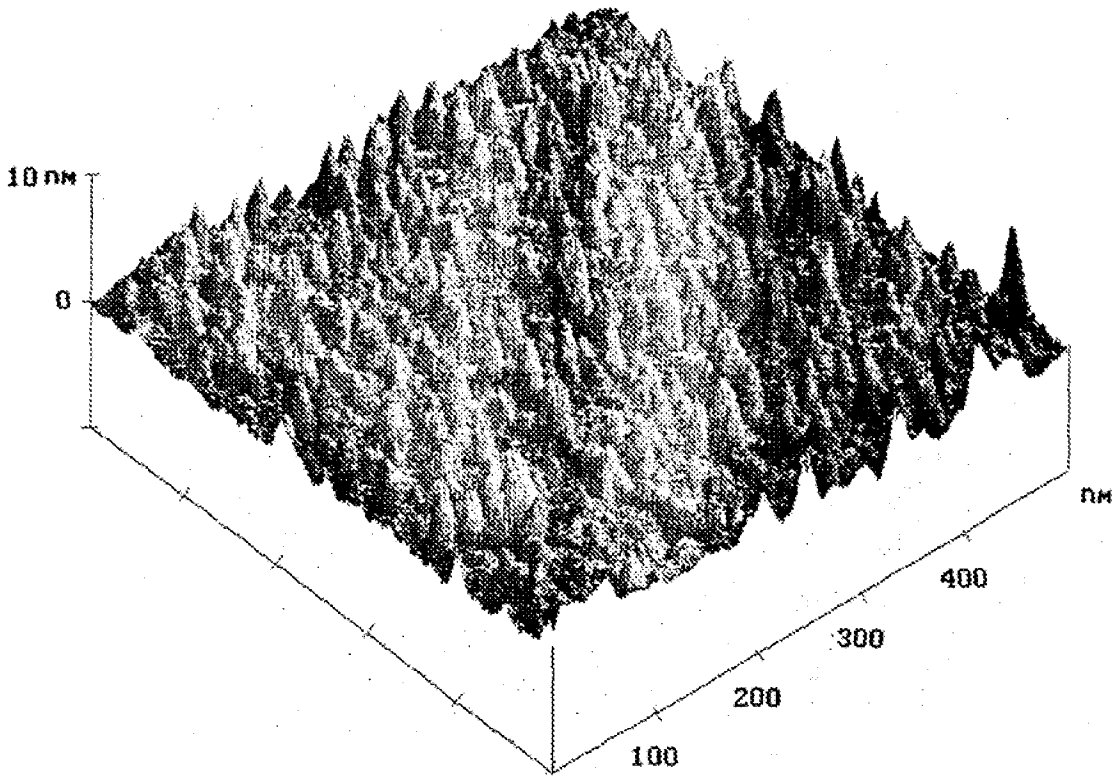


FIG. 16

(12) INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

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International Bureau

(43) International Publication Date
21 February 2002 (21.02.2002)

PCT

(10) International Publication Number
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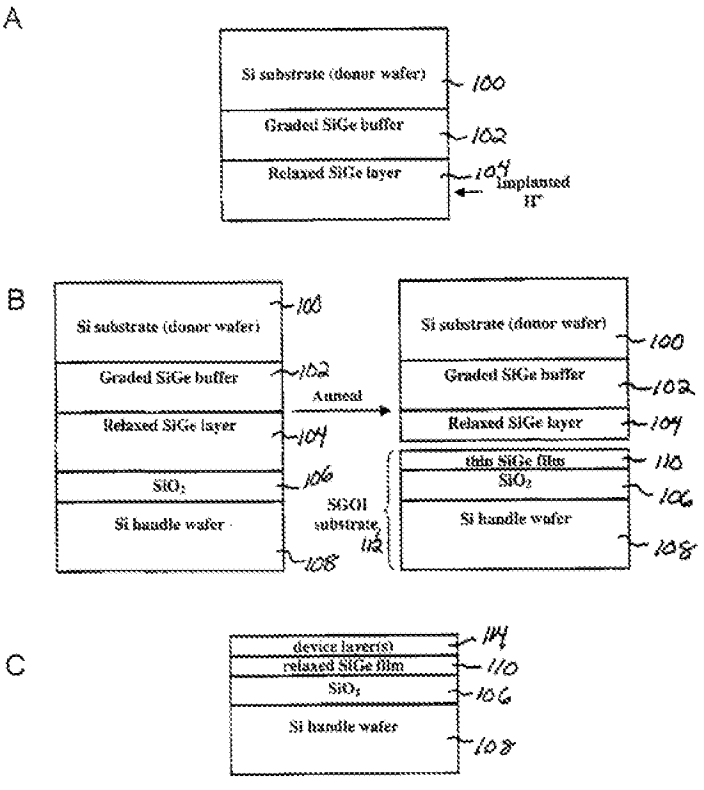

(57) Abstract: A process for producing monocrystalline semiconductor layers. In an exemplary embodiment, a graded $Si_{1-x}Ge_x$(x increases from 0 to y) is deposited on a first silicone substrate, followed by deposition of a relaxed $Si_{1-y}Ge_y$ layer, a thin strained $Si_{1-z}Ge_z$?layer. Hydrogen ions are then introduced into the strained Si_zGe_z layer. The relaxed $Si_{1-y}Ge_y$ layer is bonded to a second oxidized substrate. An annealing treatment splits the bonded pair at the strained Si layer, such that the second relaxed $Si_{1-y}Ge_y$ layer remains on the second substrate. In another exemplary embodiment, a graded $Si_{1-x}Ge_x$ is deposited on a first silicon substrate, where the Ge concentration x is increased from 0 to 1. Then a relaxed GaAs layer is deposited on the relaxed Ge buffer. As the lattice constant of GaAs is close to that of Ge, GaAs has high quality with limited dislocation defects. Hydrogen ions are introduced into the relaxed GaAs layer at the selected depth. The relaxed GaAs layer is bonded to a second oxidized substrate. An annealing treatment splits the bonded pair at the hydrogen ion rich layer, such that the upper portion of relaxed GaAs layer remains on the second substrate.

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PROCESS FOR PRODUCING SEMICONDUCTOR ARTICLE USING GRADED EXPITAXIAL GROWTH

PRIORITY INFORMATION

This application claims priority from provisional application Ser. No. 60/225,666 filed August 16, 2000.

BACKGROUND OF THE INVENTION

The present invention relates to a production of a general substrate of relaxed $Si_{1-x}Ge_x$-on-insulator (SGOI) for various electronics or optoelectronics applications, and the production of monocrystalline III-V or II-VI material-on-insulator substrate.

Relaxed $Si_{1-x}Ge_x$-on-insulator (SGOI) is a very promising technology as it combines the benefits of two advanced technologies: the conventional SOI technology and the disruptive SiGe technology. The SOI configuration offers various advantages associated with the insulating substrate, namely reduced parasitic capacitances, improved isolation, reduced short-channel-effect, etc. High mobility strained-Si, strained-$Si_{1-x}Ge_x$ or strained-Ge MOS devices can be made on SGOI substrates.

Other III-V optoelectronic devices can also be integrated into the SGOI substrate by matching the lattice constants of III-V materials and the relaxed $Si_{1-x}Ge_x$. For example a GaAs layer can be grown on $Si_{1-x}Ge_x$-on-insulator where x is equal or close to 1. SGOI may serve as an ultimate platform for high speed, low power electronic and optoelectronic applications.

SGOI has been fabricated by several methods in the prior art. In one method, the separation by implantation of oxygen (SIMOX) technology is used to produce SGOI. High dose oxygen implant was used to bury high concentrations of oxygen in a $Si_{1-x}Ge_x$ layer, which was then converted into a buried oxide (BOX) layer upon annealing at high temperature (for example, 1350 °C). See, for example, Mizuno et al. IEEE Electron Device Letters, Vol. 21, No. 5, pp. 230-232, 2000 and Ishilawa et al. Applied Physics Letters, Vol. 75, No. 7, pp. 983-985, 1999. One of the main drawbacks is the quality of the resulting $Si_{1-x}Ge_x$ film and BOX. In addition, Ge segregation during high temperature anneal also limits the maximum Ge composition to a low value.

U.S. Pat. Nos. 5,461,243 and 5,759,898 describe a second method, in which a conventional silicon-on-insulator (SOI) substrate was used as a compliant substrate. In the

process, an initially strained $Si_{1-x}Ge_x$ layer was deposited on a thin SOI substrate. Upon an anneal treatment, the strain was transferred to the thin silicon film underneath, resulting in relaxation of the top $Si_{1-x}Ge_x$ film. The final structure is relaxed-SiGe/strained-Si/insulator, which is not an ideal SGOI structure. The silicon layer in the structure is unnecessary, and may complicate or undermine the performance of devices built on it. For example, it may form a parasitic back channel on this strained-Si, or may confine unwanted electrons due to the band gap offset between the strained-Si and SiGe layer.

U.S. Pat. Nos. 5,906,951 and 6,059,895 describe the formation of a similar SGOI structure: strained-layer(s)/relaxed-SiGe/Si/insulator structure. The structure was produced by wafer bonding and etch back process using a P^{++} layer as an etch stop. The presence of the silicon layer in the above structure may be for the purpose of facilitating Si-insulator wafer bonding, but is unnecessary for ideal SGOI substrates. Again, the silicon layer may also complicate or undermine the performance of devices built on it. For example, it may form a parasitic back channel on this strained-Si, or may confine unwanted electrons due to the band gap offset between the strained-Si and SiGe layer. Moreover, the etch stop of P^{++} in the above structure is not practical when the first graded $Si_{1-y}Ge_y$ layer described in the patents has a y value of larger than 0.2. Experiments from research shows $Si_{1-y}Ge_y$ with y larger than 0.2 is a very good etch stop for both KOH and TMAH, as described in a published PCT application WO 99/53539. Therefore, the KOH will not be able to remove the first graded $Si_{1-y}Ge_y$ layer and the second relaxed SiGe layer as described in the patents.

Other attempts include re-crystallization of an amorphous $Si_{1-x}Ge_x$ layer deposited on the top of SOI (silicon-on-insulator) substrate, which is again not an ideal SGOI substrate and the silicon layer is unnecessary, and may complicate or undermine the performance of devices built on it. Note Yeo et al. IEEE Electron Device Letters, Vol. 21, No. 4, pp. 161-163, 2000. The relaxation of the resultant SiGe film and quality of the resulting structure are main concerns.

From the above, there is a need for a simple technique for relaxed SGOI substrate production, a need for a technique for production of high quality SGOI and other III-V material-on-insulator, and a need for a technique for wide range of material transfer.

SUMMARY OF THE INVENTION

According to the invention, there is provided an improved technique for production

of wide range of high quality material is provided. In particular, the production of relaxed $Si_{1-x}Ge_x$-on-insulator (SGOI) substrate or relaxed III-V or II-VI material-on-insulator, such as GaAs-on-insulator, is described. High quality monocrystalline relaxed SiGe layer, relaxed Ge layer, or other relaxed III-V material layer is grown on a silicon substrate using a graded $Si_{1-x}Ge_x$ epitaxial growth technique. A thin film of the layer is transferred into an oxidized handle wafer by wafer bonding and wafer splitting using hydrogen ion implantation. The invention makes use of the graded $Si_{1-x}Ge_x$ buffer structure, resulting in a simplified and improved process.

The invention also provides a method allowing a wide range of device materials to be integrated into the inexpensive silicon substrate. For example, it allows production of $Si_{1-x}Ge_x$-on-insulator with wide range of Ge concentration, and allows production of many III-V or II-VI materials on insulator like GaAs, AlAs, ZnSe and InGaP. The use of graded $Si_{1-x}Ge_x$ buffer in the invention allows high quality materials with limited dislocation defects to be produced and transferred. In one example, SGOI is produced using a SiGe structure in which a region in the graded buffer can act as a natural etch stop.

The invention provides a process and method for producing monocrystalline semiconductor layers. In an exemplary embodiment, a graded $Si_{1-x}Ge_x$ (x increases from 0 to y) is deposited on a first silicon substrate, followed by deposition of a relaxed $Si_{1-y}Ge_y$ layer, a thin strained $Si_{1-z}Ge_z$ layer and another relaxed $Si_{1-y}Ge_y$ layer. Hydrogen ions are then introduced into the strained $Si_{1-z}Ge_z$ layer. The relaxed $Si_{1-y}Ge_y$ layer is bonded to a second oxidized substrate. An annealing treatment splits the bonded pair at the strained Si layer, whereby the second relaxed $Si_{1-y}Ge_y$ layer remains on said second substrate.

In another exemplary embodiment, a graded $Si_{1-x}Ge_x$ is deposited on a first silicon substrate, where the Ge concentration x is increased from 0 to 1. Then a relaxed GaAs layer is deposited on the relaxed Ge buffer. As the lattice constant of GaAs is close to that of Ge, GaAs has high quality with limited dislocation defects. Hydrogen ions are introduced into the relaxed GaAs layer at the selected depth. The relaxed GaAs layer is bonded to a second oxidized substrate. An annealing treatment splits the bonded pair at the hydrogen ion rich layer, whereby the upper portion of relaxed GaAs layer remains on said second substrate.

BRIEF DESCRIPTION OF THE DRAWINGS

Figs. 1A-1C are block diagrams showing the process of producing a SGOI

substrate in accordance with the invention;

Figs. 2A and 2B are infrared transmission images of an as-bonded wafer pair and a final SGOI substrate after splitting, respectively;

Fig. 3 is a TEM cross-section view of a SiGe layer that was transferred onto the top of a buried oxide;

Fig. 4 is an AFM for a transferred SGOI substrate showing surface roughness; and

Figs. 5-8 are block diagrams of various exemplary embodiments semiconductor structures in accordance with the invention.

DETAILED DESCRIPTION OF THE INVENTION

An example of a process in which SGOI is created by layer transfer is described. The experiment was performed in two stages. In the first stage, heteroepitaxial SiGe layers are formed by a graded epitaxial growth technology. Starting with a 4-inch Si (100) donor wafer 100, a linearly stepwise compositionally graded $Si_{1-x}Ge_x$ buffer 102 is deposited with CVD, by increasing Ge concentration from zero to 25%. Then a 2.5 μm relaxed $Si_{0.75}Ge_{0.25}$ cap layer 104 is deposited with the final Ge composition, as shown in Fig. 1A.

The relaxed SiGe cap layer has high quality with very low dislocation defect density (less than 1E6 /cm^2), as the graded buffer accommodates the lattice mismatch between Si and relaxed SiGe. A thin layer of this high quality SiGe will be transferred into the final SGOI structure. The surface of the as-grown relaxed SiGe layer shows a high roughness around 11nm to 15nm due to the underlying strain fields generated by misfit dislocations at the graded layer interfaces and thus chemical-mechanical polishing (CMP) is used to smooth the surface. In the second stage, the donor wafer is implanted with hydrogen ion (100 keV, 5E16 H^+/cm^2) to form a buried hydrogen-rich layer. After a surface clean step in a modified RCA solution, it is bonded to an oxidized 106 Si handle wafer 108 at room temperature as shown in Fig. 1B.

The wafer bonding is one of the key steps, and the bonding energy should be strong enough in order to sustain the subsequent layer transfer in the next step. Good bonding requires a flat surface and a highly hydrophilic surface before bonding. On the other hand, the buried oxide in the final bonded structure is also required to have good electrical properties as it will influence the final device fabricated on it. In the conventional Si film transfer, thermal oxide on the donor wafer is commonly used before H^+ implantation and wafer bonding, which becomes the buried oxide in the

resulting silicon-on-insulator structure.

The thermal oxide of the Si donor wafer meets all the requirements, as it has good electrical properties, has flat surface and bonds very well to the handle wafer. Unlike the Si, however, the oxidation of SiGe film results in poor thermal oxide quality, and the Ge segregation during oxidation also degrades the SiGe film. Therefore the thermal oxide of SiGe is not suitable for the SGOI fabrication. In one exemplary experiment the SiGe film will be directly bonded to an oxidized Si handle wafer. The high quality thermal oxide in the handle wafer will become the buried oxide in the final SGOI structure.

Having a flat surface after a CMP step, the SiGe wafer went through a clean step. Compared to Si, one difficulty of SiGe film is that, SiGe surface becomes rougher during the standard RCA clean, as the NH_4OH in RCA1 solution etches Ge faster than Si. Rough surface will lead to weak bonding as the contact area is reduced when bonded to the handle wafer. In this exemplary embodiment, H_2SO_4-H_2O_2 solution is used in the place of RCA1, which also meets the clean process requirement for the subsequent furnace annealing after bonding. The SiGe surface after H_2SO_4-H_2O_2 clean shows better surface roughness compared to RCA1.

After this modified clean procedure, the SiGe wafer is dipped in the diluted HF solution to remove the old native oxide. It is then rinsed in DI water thoroughly to make the surface hydrophilic by forming a fresh new native oxide layer that is highly active. After spinning dry, the SiGe wafer is bonded to an oxidized handle wafer at room temperature, and then annealed at 600 °C for 3 hours. During anneal the bonded pair split into two sheets along the buried hydrogen-rich layer, and a thin relaxed $Si_{0.75}Ge_{0.25}$ film 110 is transferred into the handle wafer, resulting in a SGOI substrate 112, as shown in Fig. 1B. A final 850 °C anneal improves the $Si_{0.75}Ge_{0.25}/SiO_2$ bond. Thereafter, device layers 114 can be processed on the SGOI substrate 112 as shown in Fig. 1C.

Figs. 2A and 2B are infrared transmission images of the as-bonded wafer pair and the final SGOI substrate after splitting, respectively. To investigate the surface of the as-transferred SGOI substrate, transmission electron microscopy (TEM) and atomic force microscopy (AFM) were used. The TEM cross-section view in Fig. 3 shows a ~640 nm SiGe layer was transferred onto the top of a 550 nm buried oxide (BOX). Surface damage is also shown clearly at the splitting surface with a damage depth of ~100 nm.

Fig. 4 shows a surface roughness of 11.3 nm in an area of 5x5 μm^2 by AFM for the

as-transferred SGOI. The data is similar to those from as-transferred silicon film by smart-cut process, and suggests that a top layer of about 100 nm should be removed by a final CMP step.

After SiGe film transferring, only a thin relaxed SiGe film is removed and the donor wafer can be used again for a donor wafer. Starting from this general SGOI substrate, various device structures can be realized by growing one or more device layers on the top, as shown in Fig. 2C. Electrical evaluation is in progress by growing a strain Si layer on the top of this SGOI substrate followed by fabrication of strained Si channel devices.

Bond strength is important to the process of the invention. AFM measurements were conducted to investigate the SiGe film surface roughness before bonding under different conditions. One experiment is designed to investigate how long the SiGe surface should be polished to have smooth surface and good bond strength, since the surface of the as-grown relaxed SiGe layer has a high roughness around 11nm to 15nm. Several identical 4-inch Si wafers with relaxed $Si_{0.75}Ge_{0.25}$ films were CMPed with optimized polishing conditions for different times. Using AFM, the measured surface mircoroughness RMS at an area of 10μm x 10μm is 5.5Å, 4.5Å and 3.8Å, for wafer CMPed for 2 min., 4 min. and 6 min. respectively. After bonding to identical handle wafers, the tested bond strength increases with decreasing RMS. A CMP time of 6 min. is necessary for good strength.

In another experiment, two identical 4-inch Si wafers with relaxed $Si_{0.75}Ge_{0.25}$ films were CMPed for 8 min. After two cleaning steps in H_2SO_4:H_2O_2 solution and one step in diluted HF solution, one wafer was put in a new H_2SO_4:H_2O_2 (3:1) solution and another in a new NH_4OH:H_2O_2:H_2O (1:1:5), i.e. the conventional RCA1 solution, both for 15 min. The resultant wafers were tested using AFM. The wafer after H_2SO_4:H_2O_2 solution shows a surface roughness RMS of 2Å at an area of 1μm x 1μm, which after NH_4OH:H_2O_2:H_2O shows 4.4Å. Clearly, the conventional RCA clean roughens the SiGe surface significantly, and H_2SO_4:H_2O_2 should be used for SiGe clean.

In yet another experiment, the clean procedure is optimized before bonding. For direct SiGe wafer to oxidized handle wafer bonding (SiGe-oxide bonding), several different clean procedures were tested. It has been found that the H_2SO_4:H_2O_2 (2~4:1) solution followed by DI water rinse and spin dry gives good bond strength. Alternatively, one can also deposit an oxide layer on the SiGe wafer and then CMP the oxide layer. In this case, SiGe/oxide is bonded to an oxidized handle wafer, i.e. oxide-oxide bonding. Among different clean procedures, it was found that NH_4OH:H_2O_2:H_2O clean and DI

water rinse following by diluted HF, DI water rinse and spin dry gives very good bond strength.

Fig. 5 is a block diagram of an exemplary embodiment of a semiconductor structure 500 in accordance with the invention. A graded $Si_{1-x}Ge_x$ buffer layer 504 is grown on a silicon substrate 502, where the Ge concentration x is increased from zero to a value y in a stepwise manner, and y has a selected value between 0 and 1. A second relaxed $Si_{1-y}Ge_y$ layer 506 is then deposited, and hydrogen ions are implanted into this layer with a selected depth by adjusting implantation energy, forming a buried hydrogen-rich layer 508. The wafer is cleaned and bonded to an oxidized handle wafer 510. An anneal treatment at 500~600°C splits the bonded pair at the hydrogen-rich layer 508. As a result, the upper portion of the relaxed $Si_{1-y}Ge_y$ layer 506 remains on the oxidized handle wafer, forming a SGOI substrate. The above description also includes production of Ge-on-insulator where y = 1.

During the wafer clean step prior to bonding, the standard RCA clean for the silicon surface is modified. Since the NH_4OH in standard RCA1 solution etches Ge faster than Si, the SiGe surface will become rough, leading to a weak bond. A H_2SO_4-H_2O_2 solution is used in the place of RCA1, which also meets the clean process requirement for the subsequent furnace annealing after bonding. The SiGe surface after the H_2SO_4-H_2O_2 clean showed better surface roughness compared to RCA1. After the modified RCA clean, the wafers are then immersed in another fresh H_2SO_4-H_2O_2 solution for 10 to 20 min. H_2SO_4-H_2O_2 renders the SiGe surface hydrophilic. After a rinse in DI wafer and spin drying, the SiGe wafer is bonded to an oxidized handle wafer at room temperature immediately, and then annealed at 500~600°C for wafer splitting.

Fig. 6 is a block diagram of another exemplary embodiment of a semiconductor structure 600. The structure 600 includes a graded $Si_{1-x}Ge_x$ buffer layer 604 grown on a silicon substrate 602, where the Ge concentration x is increased from zero to 1. Then a relaxed pure Ge layer 606 and a III-V material layer 608, such as a GaAs layer, are epitaxially grown on the Ge layer. Hydrogen ions are implanted into the GaAs layer 608 with a selected depth by adjusting implantation energy, forming a buried hydrogen-rich layer 610. The wafer is cleaned and bonded to an oxidized handle wafer 612. An anneal treatment splits the bonded pair at the hydrogen-rich layer 610. As a result, the upper portion of the GaAs layer 608 remains on the oxidized handle wafer, forming a GaAs-on-insulator substrate.

Fig. 7. is a block diagram of yet another exemplary embodiment of a

semiconductor structure 700. A graded $Si_{1-x}Ge_x$ buffer layer 704 is grown on a silicon substrate 702, where the Ge concentration x is increased from zero to a selected value y, where y is less than 0.2. A second relaxed $Si_{1-z}Ge_z$ layer 706 is deposited, where z is between 0.2 to 0.25. Hydrogen ions are implanted into the graded $Si_{1-x}Ge_x$ buffer layer 704 with a selected depth, forming a buried hydrogen-rich layer 708 within layer 704. The wafer is cleaned and bonded to an oxidized handle wafer 710. An anneal treatment at 500~600C° splits the bonded pair at the hydrogen-rich layer 708.

As a result, the upper portion of the graded $Si_{1-x}Ge_x$ buffer layer 704 and the relaxed $Si_{1-z}Ge_z$ layer 706 remains on the oxidized handle wafer 710. The remaining graded $Si_{1-x}Ge_x$ buffer layer 704 is then selectively etched by either KOH or TMAH. KOH and TMAH etch $Si_{1-x}Ge_x$ fast when x is less 0.2, but becomes very slow when x is larger than 0.2. Thus, the graded $Si_{1-x}Ge_x$ buffer layer 704 can be etched selectively, leaving the relaxed $Si_{1-z}Ge_z$ layer 706 on the insulating substrate 710 and forming a relaxed SGOI substrate. In this process, the thickness of the relaxed $Si_{1-z}Ge_z$ film 706 on the final SGOI structure is defined by film growth, which is desired in some applications.

Fig. 8 is a block diagram of yet another exemplary embodiment of a semiconductor structure 800. A graded $Si_{1-x}Ge_x$ buffer layer 804 is grown on a silicon substrate 802, where the Ge concentration x is increased from zero to a selected value y between 0 and 1. A second relaxed $Si_{1-y}Ge_y$ layer 806 is deposited, followed by a strained $Si_{1-z}Ge_z$ layer 808 and another relaxed $Si_{1-y}Ge_y$ layer 810. The thickness of layers 806, 808, and 810, and the value z are chosen such that the $Si_{1-z}Ge_z$ layer 808 is under equilibrium strain state while the $Si_{1-y}Ge_y$ layers 806 and 810 remain relaxed. In one option, hydrogen ions may be introduced into the strained $Si_{1-z}Ge_z$ layer 808, forming a hydrogen-rich layer 812. The wafer is cleaned and bonded to an oxidized handle wafer 814. The bonded pair is then separated along the strained $Si_{1-z}Ge_z$ layer 808.

Since the strain makes the layer weaker, the crack propagates along this layer during separation. The separation can be accomplished by a variety of techniques, for example using a mechanical force or an anneal treatment at 500~600C° when the hydrogen is also introduced. See, for example, U.S. Pat. Nos. 6,033,974 and 6,184,111, both of which are incorporated herein by reference. As a result, the relaxed $Si_{1-y}Ge_y$ layer 810 remains on the oxidized handle wafer, forming a relaxed SGOI substrate. The thickness of layers 806, 808, and 810, and the value z may also be chosen such that there are a good amount of dislocations present in the $Si_{1-z}Ge_z$ layer 808 while the top $Si_{1-y}Ge_y$ layer 810

remains relaxed and having high quality and limited dislocation defects.

These dislocation defects in the $Si_{1-z}Ge_z$ layer 808 can then act as hydrogen trap centers during the subsequent step of introducing ions. The hydrogen ions may be introduced by various ways, such as ion implantation or ion diffusion or drift by means of electrolytic charging. The value of z may be chosen in such a way that the remaining $Si_{1-z}Ge_z$ layer 808 can be etched selectively by KOH or TMAH. The layers 806 and 810 may also be some other materials, for example pure Ge, or some III-V materials, under the condition that the Ge concentration x in the graded $Si_{1-x}Ge_x$ buffer layer 804 is increased from zero to 1.

After all the semiconductor-on-insulator substrate obtained by the approaches described above, various device layers can be further grown on the top. Before the regrowth, CMP maybe used to polish the surface.

Although the present invention has been shown and described with respect to several preferred embodiments thereof, various changes, omissions and additions to the form and detail thereof, may be made therein, without departing from the spirit and scope of the invention.

What is claimed is:

CLAIMS

1. A process of forming a semiconductor structure with a relaxed $Si_{1-y}Ge_y$ layer, comprising:

depositing a graded $Si_{1-x}Ge_x$ buffer layer on a first substrate, wherein said Ge concentration x is increased from zero to a value y;

depositing a relaxed $Si_{1-y}Ge_y$ layer;

introducing ions into said relaxed $Si_{1-y}Ge_y$ layer to define a first heterostructure;

bonding said first heterostructure to a second substrate to define a second heterostructure;

splitting said second heterostructure in the region of the introduced ions, wherein a top portion of said relaxed $Si_{1-y}Ge_y$ layer remains on said second substrate.

2. The process of claim 1 further comprising forming at least one device layer or a plurality of integrated circuit devices, after said step of depositing said relaxed $Si_{1-y}Ge_y$ layer.

3. The process of claim 2, wherein said at least one device layer comprises at least one of strained Si, strained $Si_{1-w}Ge_w$ with $w \neq y$, strained Ge, GaAs, AlAs, ZnSe and InGaP.

4. The process of claim 1 further comprising forming an insulating layer before said step of introducing ions.

5. The process of claim 1 further comprising planarizing said relaxed $Si_{1-y}Ge_y$ layer, before said step of introducing ions.

6. The process of claim 1, wherein said ions comprise hydrogen H^+ ions or H_2^+ ions.

7. The process of claim 1 further comprising planarizing said relaxed $Si_{1-y}Ge_y$ layer, after said step of introducing ions.

8. The process of claim 1 further comprising cleaning both said first heterostructure and said second substrate, before said step of bonding.

9. The process of claim 1, wherein said second heterostructure is split by annealing.

10. The process of claim 1, wherein said second heterostructure is split by annealing followed by mechanical force.

11. The process of claim 1 further comprising removing the top portion of the remaining of said relaxed $Si_{1-y}Ge_y$ layer, after said step of splitting.

12. The process of claim 1 further comprising forming at least one device layer, or a plurality of integrated circuit devices, after said step of splitting.

13. The process of claim 12, wherein said at least one device layer comprises at least one of relaxed $Si_{1-y}Ge_y$, strained Si, strained $Si_{1-w}Ge_w$, strained Ge, GaAs, AlAs, ZnSe and InGaP.

14. The process of claim 1 further comprising re-using the remaining first heterostructure, after said step of splitting.

15. The process of claim 1, wherein said first substrate comprises monocrystalline silicon.

16. A process of forming a semiconductor layer, comprising:

depositing a graded $Si_{1-x}Ge_x$ buffer layer on a first substrate, said Ge concentration x being increased from zero to 1;

depositing a relaxed Ge layer;

forming a monocrystalline semiconductor layer including another material whose lattice constant is approximately close to that of Ge;

introducing ions into said semiconductor layer to define a first heterostructure;

bonding said first heterostructure to a second substrate to define a second heterostructure;

splitting said second heterostructure in the region of introduced ions, wherein a top portion of said semiconductor layer remains on said second substrate.

17. The process of claim 16, wherein said semiconductor layer comprises one of GaAs, AlAs, ZnSe and InGaP.

18. The process of claim 16 further comprising forming at least one device layer or a plurality of integrated circuit devices, after said step of forming said semiconductor layer.

19. The process of claim 16 further comprising forming an insulating layer before said step of introducing ions.

20. The process of claim 16 further comprising planarizing said semiconductor layer before said step of introducing ions.

21. The process of claim 16, wherein said ions comprise hydrogen H^+ ions or H_2^+ ions.

22. The process of claim 16, further comprising the step of planarizing said semiconductor layer after said step of introducing ions.

23. The process of claim 16 further comprising cleaning both said first heterostructure and said second substrate, before said step of bonding.

24. The process of claim 16, wherein said second heterostructure is split by annealing.

25. The process of claim 16, wherein said second heterostructure is split by annealing and followed by mechanical force.

26. The process of claim 16 further comprising removing the top portion of the remaining of said third semiconductor layer, after said step of splitting.

27. The process of claim 16 further comprising forming at least one device layer or a plurality of integrated circuit devices, after said step of splitting.

28. The process of claim 16 further comprising re-using the remaining first heterostructure, after said step of splitting.

29. The process of claim 16, wherein said first substrate comprises monocrystalline silicon.

30. A process of forming a semiconductor structure with a relaxed $Si_{1-z}Ge_z$ layer, comprising:

depositing a graded $Si_{1-x}Ge_x$ buffer layer on a first substrate, said Ge concentration x being increased from zero to a selected value y, and y being less than 0.2;

depositing a relaxed $Si_{1-z}Ge_z$ layer, where z is between 0.2 and 0.25;

introducing ions into said graded $Si_{1-x}Ge_x$ buffer layer to define a first heterostructure;

bonding said first heterostructure to a second substrate to define a second heterostructure;

splitting said second heterostructure in the region of introduced ions, wherein the upper portion of first graded $Si_{1-x}Ge_x$ layer and said relaxed $Si_{1-z}Ge_z$ layer remains on said second substrate; and

selectively etching the remaining portion of said graded $Si_{1-x}Ge_x$ layer, wherein said relaxed $Si_{1-z}Ge_z$ layer remains on said second substrate.

31. The process of claim 30 further comprising forming at least one device layer or a plurality of integrated circuit devices, after said step of forming said relaxed $Si_{1-z}Ge_z$ layer.

32. The process of claim 31, wherein said at least one device layer includes one or more of strained Si, strained $Si_{1-w}Ge_w$ with $w \neq z$, and strained Ge.

33. The process of claim 30 further comprising forming an insulating layer before said step of introducing ions.

34. The process of claim 30 further comprising planarizing said relaxed $Si_{1-z}Ge_z$ layer before said step of introducing ions.

35. The process of claim 30, wherein said ions comprise hydrogen H^+ ions or H_2^+ ions.

36. The process of claim 30 further comprising planarizing the relaxed $Si_{1-z}Ge_z$ layer after said step of introducing ions.

37. The process of claim 30 further comprising cleaning both said first heterostructure and said second substrate, before said step of bonding.

38. The process of claim 30, wherein said second heterostructure is split by annealing.

39. The process of claim 30 further comprising planarizing said second relaxed $Si_{1-z}Ge_z$ layer after said step of etching.

40. The process of claim 30 further comprising forming at least one device layer or a plurality of integrated circuit devices, after said step of etching.

41. A process of forming a semiconductor layer, comprising:

depositing a graded $Si_{1-x}Ge_x$ buffer layer on a first substrate, said Ge concentration x being increased from zero to a value y;

depositing a relaxed $Si_{1-y}Ge_y$ layer;

depositing a strained or defect layer;

depositing a relaxed layer;

introducing ions into said strained or defect layer to define a first heterostructure;

bonding said first heterostructure to a second substrate to define a second heterostructure; and

splitting said second heterostructure in the region of the strained or defect layer, wherein said relaxed layer remains on said second substrate.

42. The process of claim 41, wherein said strained or defect layer comprises either a strained $Si_{1-z}Ge_z$ layer with $z \neq y$, or other III-V material.

43. The process of claim 41, wherein said relaxed layer or said strained or defect layer comprises either a relaxed $Si_{1-w}Ge_w$ layer where w is close or equal to y, or, when y is equal to 1, one of Ge, GaAs, AlAs, ZnSe and InGaP.

44. The process of claim 41 further comprising forming at least one device layer or a plurality of integrated circuit devices, after said step of depositing said relaxed layer.

45. The process of claim 41 further comprising forming an insulating layer before said step of introducing ions.

46. The process of claim 41 further comprising planarizing said relaxed layer before said step of introducing ions.

47. The process of claim 41, wherein said ions comprise hydrogen H^+ ions or H_2^+ ions.

48. The process of claim 41 further comprising planarizing said relaxed layer after said step of introducing ions.

49. The process of claim 41 further comprising cleaning both said first heterostructure and said second substrate, before said step of bonding.

50. The process of claim 41, wherein said second heterostructure is split by annealing.

51. The process of claim 41 further comprising removing one of any remaining of said strained or defect layer, and the top portion of said relaxed layer, after said step of splitting.

52. The process of claim 41 further comprising forming at least one device layer or a plurality of integrated circuit devices, after said step of splitting.

53. The process of claim 41 further comprising re-using the remaining first heterostructure for a subsequent process after planarizing.

54. A semiconductor structure comprising:

a first semiconductor substrate;

a second layer of relaxed $Si_{1-x}Ge_x$, wherein x = 0.1 to 1; and

a third layer comprising at least one of GaAs, AlAs, ZnSe and InGaP, or strained $Si_{1-y}Ge_y$ wherein $y \neq x$.

55. A semiconductor structure comprising:

a first substrate comprising monocrystalline silicon substrate;

a second layer of graded $Si_{1-x}Ge_x$ buffer layer, wherein said Ge concentration x is increased from zero to a value y;

a third layer of relaxed $Si_{1-y}Ge_y$;

a fourth strained or defect layer comprising either a strained $Si_{1-z}Ge_z$ layer with $z \neq y$, or other III-V or II-VI material; and

a fifth relaxed layer comprising either a relaxed $Si_{1-w}Ge_w$ layer where w is close or equal to y, or, when y is equal to 1, at least one of Ge, GaAs, AlAs, ZnSe and InGaP.

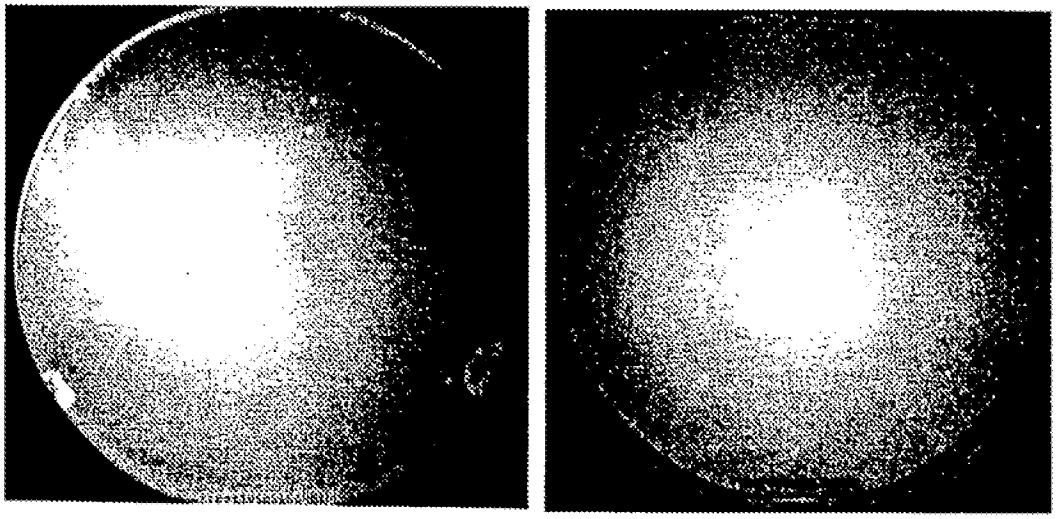


Fig. 2A

Fig. 2B

Fig. 1A

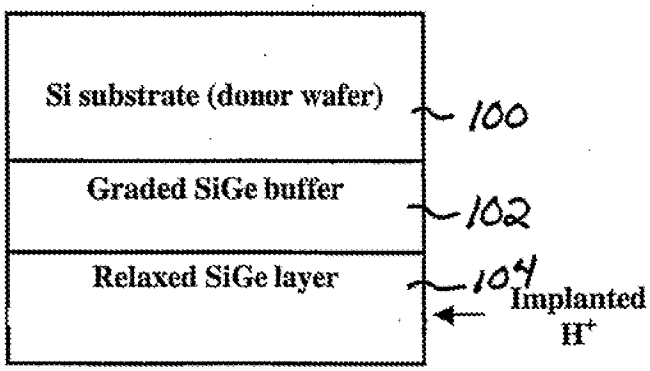


Fig. 1B

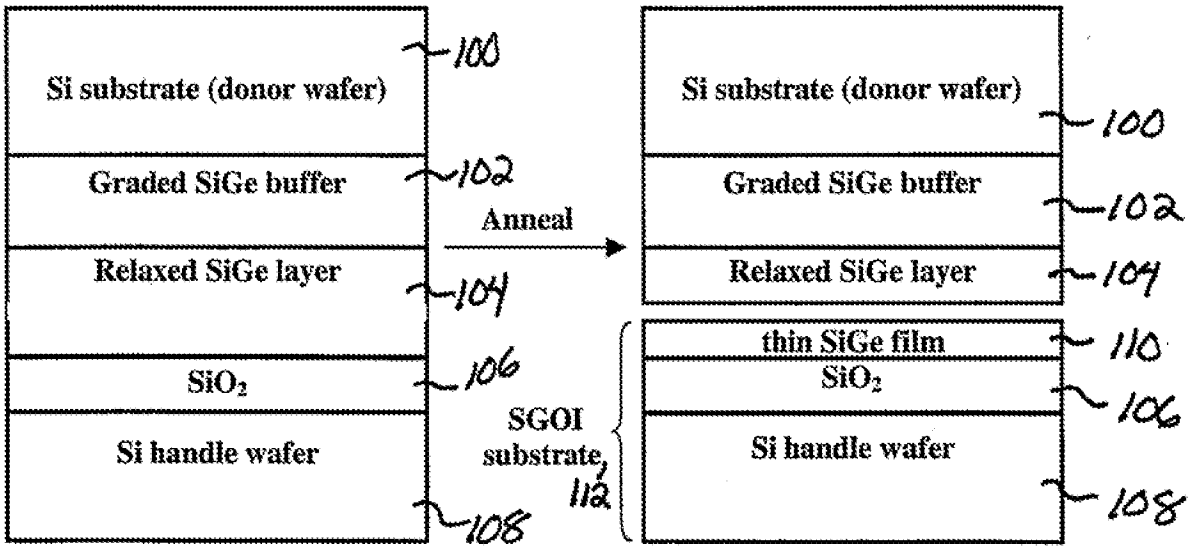


Fig. 1C

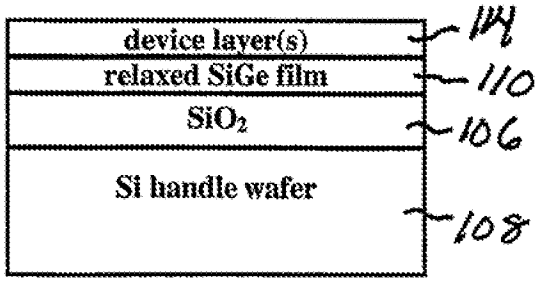


Fig. 3

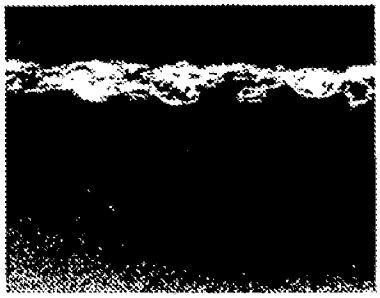

splitting surface
25% relaxed SiGe
(~ 640 nm)
BOX (550 nm)
Si (100)
200 nm

Fig. 4

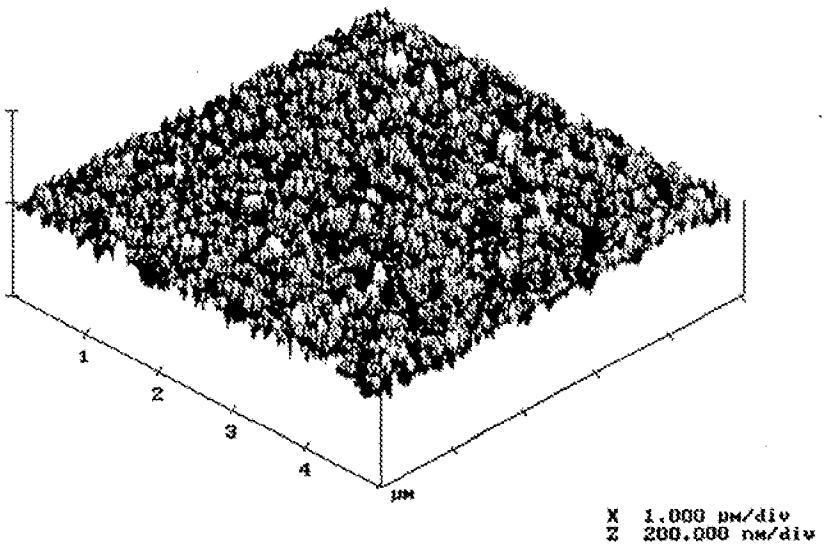


Fig. 5

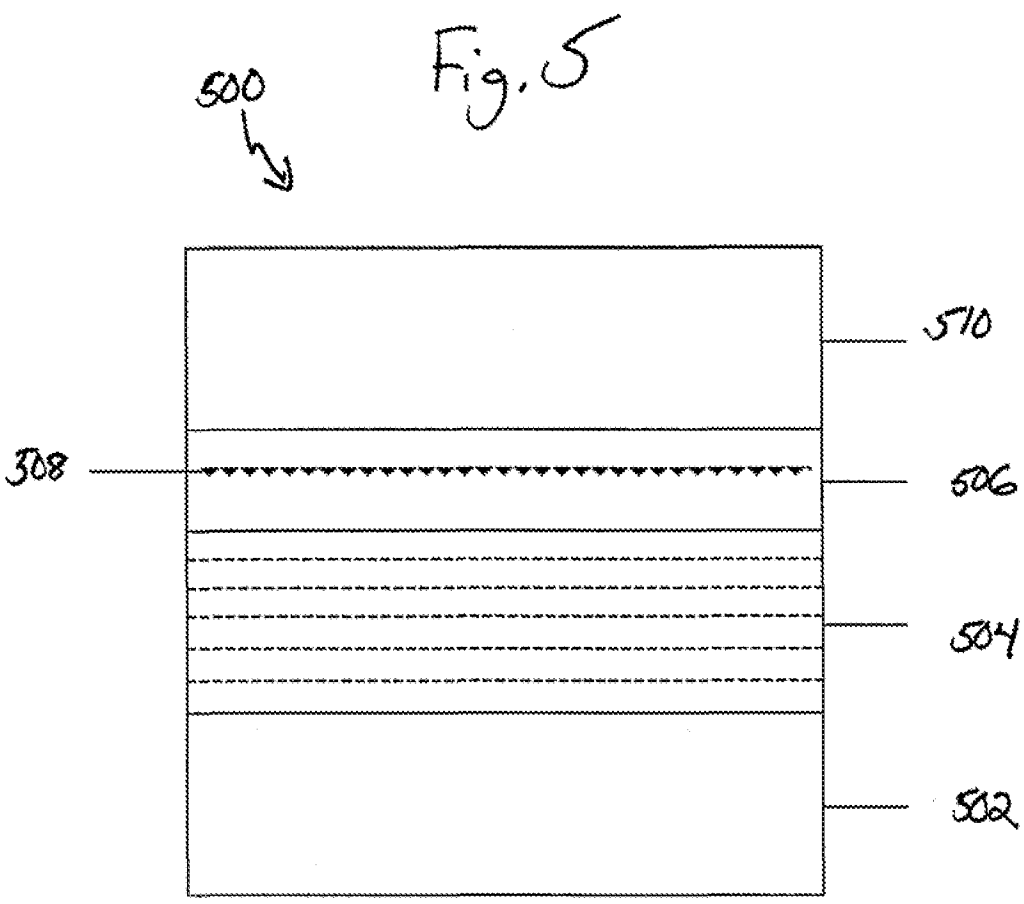


Fig. 6

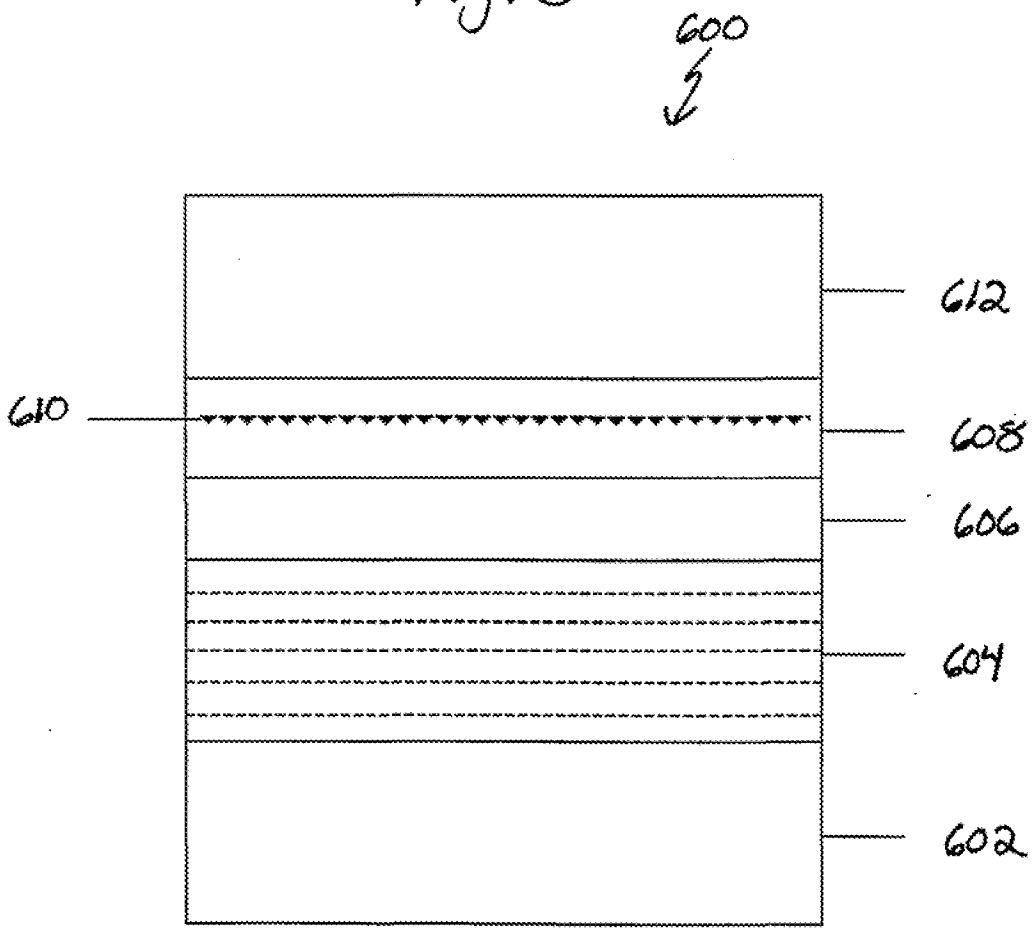


Fig. 7

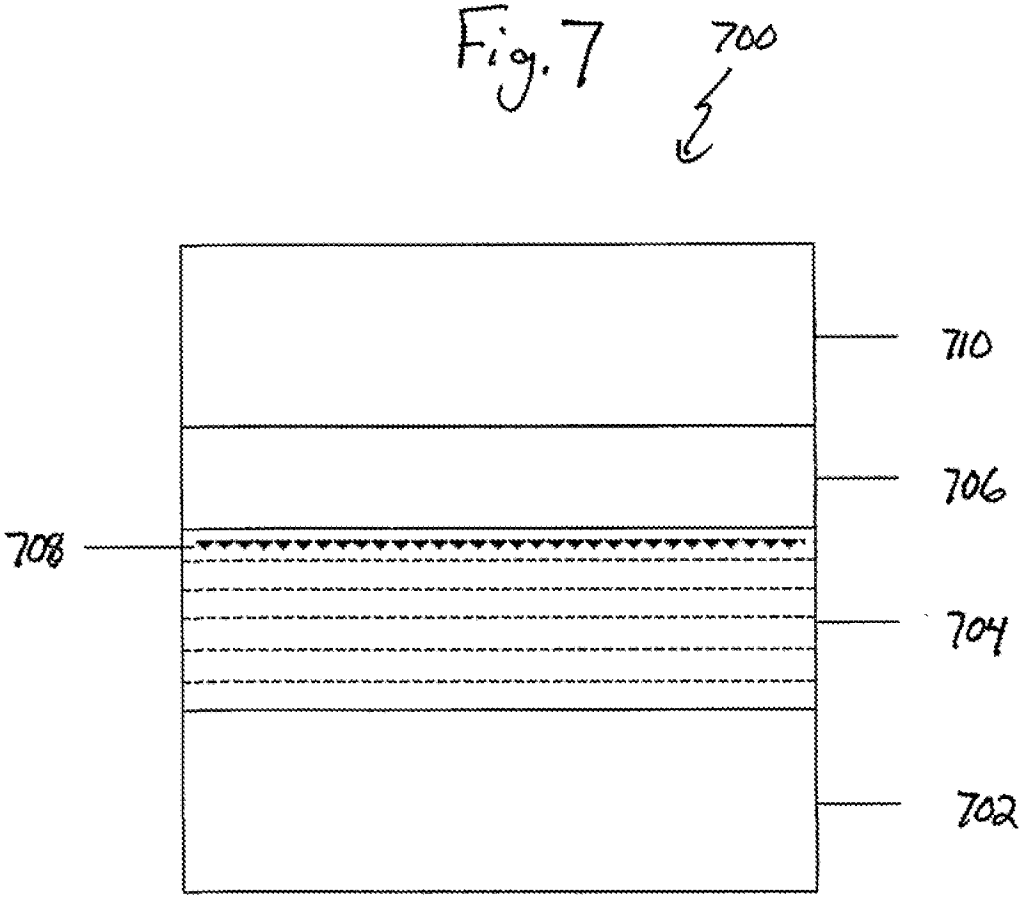
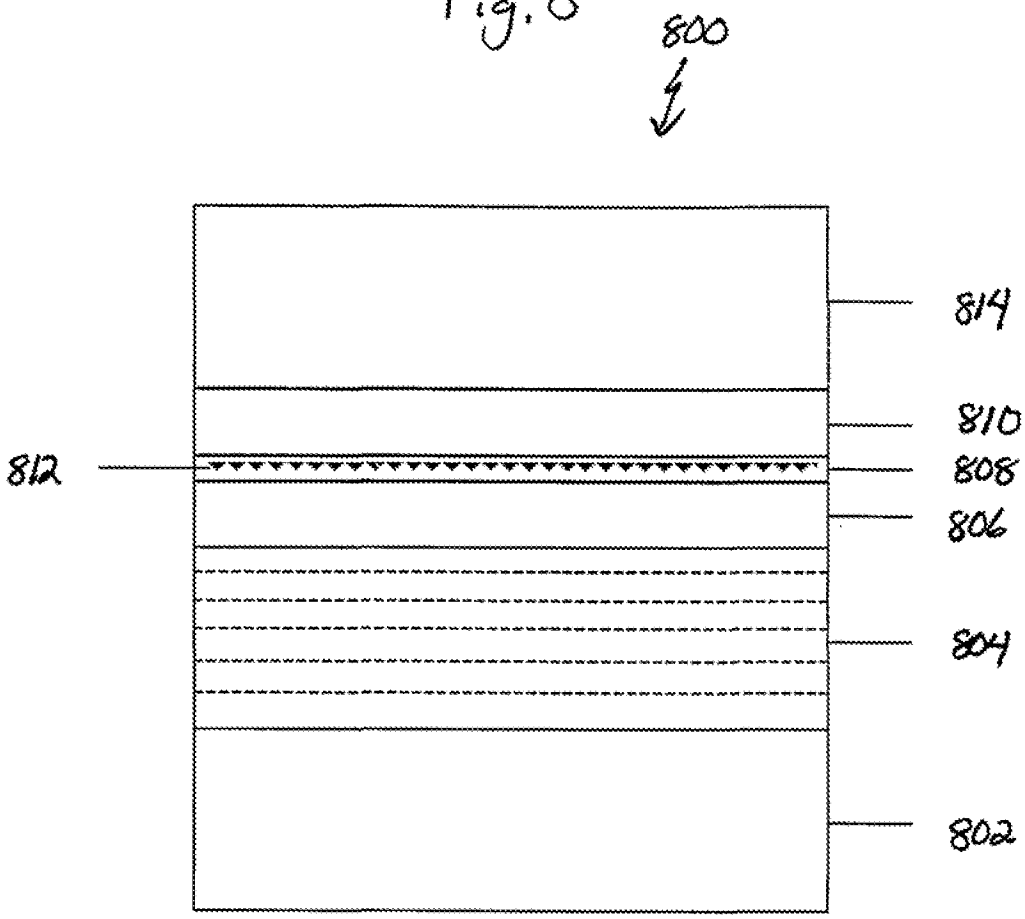


Fig. 8



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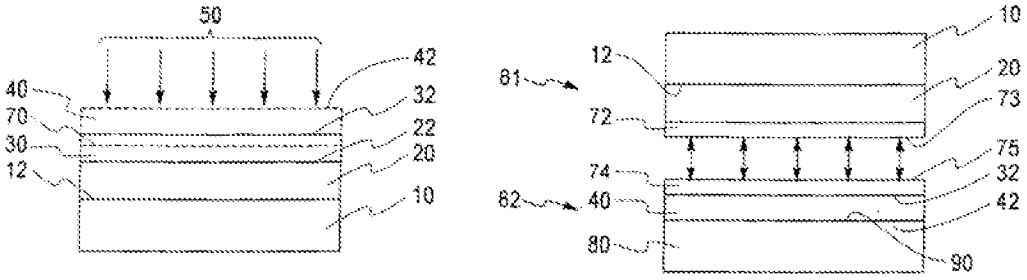
(54) Title: PREPARATION OF A RELAXED SiGe LAYER ON AN INSULATOR



(57) Abstract: A method for forming strained Si or SiGe on relaxed SiGe on insulator (74) (SGOI) is described incorporating growing a graded Si_{1-x} Ge_x layer (20) and an epitaxial Si_{1-y} Ge_y layer on a semiconductor substrate, implanting hydrogen (70) into said Si_{1-y} Ge_y layer (30) to form a hydrogen-rich defective layer, smoothing surfaces by Chemo-Mechanical Polishing, bonding two substrates together via thermal treatments and separating the two bonded substrates at the hydrogen-rich defective layer. The separated substrates may have its upper surface (75) smoothed by CMP for epitaxial deposition of further layer.

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PREPARATION OF A RELAXED SiGe LAYER ON AN INSULATOR

FIELD OF INVENTION

This invention relates to a method of preparing an SiGe layer on an insulator to provide a structure which is useful for fabricating high speed devices such as complementary metal-oxide-semiconductor (CMOS) transistors, modulation-doped field-effect-transistors (MODFETs), high electron mobility transistors (HEMTs) and bipolar transistors.

BACKGROUND OF THE INVENTION

Electron mobility in strained Si/SiGe channels is significantly higher than that in bulk Si. For example, measured values of electron mobility in strained Si at room temperature are about 3000 cm^2/Vs as opposed to 400 cm^2/Vs in bulk Si. Similarly, hole mobility in strained SiGe with high Ge concentration (60%~80%) reaches up to 800 cm^2/Vs, the value of which is about 5 times the hole mobility in bulk Si of 150 cm^2/Vs. The use of strained crystalline materials in state-of-the-art Si devices is expected to result in much higher performances, higher operating speeds in particular. Strained Si/SiGe is of particular significance when conventional Si devices continue to scale down to 0.1mm regime and start to approach the fundamental limits of unstrained materials.

However, the underlying conducting substrate for MODFETs and bipolar transistors or the interaction of the underlying substrate with the active device regions in CMOS are undesirable features which limit the full performance of high speed devices. To resolve the problem, in Si technology, an insulating layer is usually used to isolate the active device region from the substrate before creating Silicon-On-Insulator (SOI) materials to replace bulk Si material for device fabrication. Available technology to achieve SOI wafers includes Separation by Implanted Oxygen (SIMOX), bonding and etchback Silicon-On-Insulator (BESOI), separation by implanted hydrogen also known as the Smart-Cut® process which is described in U.S. Pat. No. 5,374,564 by M. Bruel which issued Dec. 20, 1994, or the combination of the last two processes for making ultra-thin SOI, U.S. Pat. No. 5,882,987 by K.V. Srikrishnan which issued Mar. 16, 1999.

When Si is substituted by strained Si/SiGe layers for high speed applications, there is a need for techniques capable of providing SiGe on insulator substrates or wafers for the fabrication of strained Si/SiGe on insulator materials. In U.S. Pat. No. 5,906,951 by Chu et al. which issued May 25, 1999, a method of utilizing wafer bonding and backside etching in KOH with a p^{++}-doped SiGe etch-stop to form a layer of strained Si/SiGe on a SOI substrate was described. However, the etch-stop layer is heavily doped by boron in the range from $5x10^{19}$ to $5x10^{20}$ atoms/cm^3 and therefore there are chances of the boron auto-doping the strained Si/SiGe layers during thermal treatment. Furthermore, the strained Si/SiGe layer may also be subjected to unwanted KOH etching if etching could not stop uniformly at the p^{++} SiGe etchstop layer due to variation of dopants in the p^{++} layer.

Another available technique for making SiGe-On-Insulator is via SIMOX as reported in a publication by T. Mizuno et al. entitled "High Performance Strained-Si p-MOSFETs on SiGe-on-Insulator Substrates Fabricated by SIMOX Technology," IEDM Technical Digest, 99-934, 1999. However, this method has limited applications because the oxygen implantation induces further damage in the relaxed SiGe layer in addition to the existing defects caused by lattice mismatch, which may consequently degrade the quality of the grown strained Si/SiGe. And, the high temperature anneal (>1100°C) needed to form oxide after the oxygen implantation is detrimental to the strained Si/SiGe layers since Ge tends to diffuse and agglomerate at temperatures above 600°C, this effect becomes more significant when the Ge content is higher than 10%. Furthermore, in this method, the insulator is limited to SiO_2 which has lower thermal conductivity compared to other insulators such as Al_2O_3.

Therefore, there is a need for an improved method for forming a structure suitable for growing strained epitaxial layers thereon.

SUMMARY OF THE INVENTION

This need is met by the invention claimed in claim 1.

In accordance with a preferred embodiment of the present invention, a method for forming a substrate suitable for growing high quality strained Si/SiGe layers on an insulator (SGOI) is described. This approach comprises the steps of selecting a first semiconductor substrate, forming

a first expitaxial graded layer of $Si_{1-x}Ge_x$ over the first semiconductor substrate, forming a second relaxed $Si_{1-y}Ge_y$ layer over the first graded layer, introducing hydrogen into the relaxed $Si_{1-y}Ge_y$ layer creating a hydrogen-rich defective layer comprising high density point defects and micro-cracks, the defective layer being within the relaxed $Si_{1-y}Ge_y$ layer, smoothing the surface of the relaxed SiGe epitaxial layer, selecting a second substrate having a layer of insulator such as SiO_2, Si_3N_4, Al_2O_3, or other acceptable or qualified low-k insulating materials, etc, on the second substrate, and having a planarized major surface on the second substrate, bonding the major surface of the first substrate to the major surface of the second substrate including the step of annealing to form a joined substrate pair with an insulator layer therein between, applying thermal treatments to the substrate pair to induce separation at the hydrogen-rich defective layer, the separation occurring to form a first structure containing the first substrate and a second structure containing the second substrate with a relaxed $Si_{1-y}Ge_y$ layer on insulator. The embodiment further includes smoothing the upper surface of the relaxed $Si_{1-y}Ge_y$ layer on said second substrate whereby the second structure is suitable for subsequent epitaxial growth of strained Si/SiGe layers for MOSFET, MODFET, HEMT or bipolar transistor device applications.

BRIEF DESCRIPTION OF THE DRAWING

Embodiments of the invention will now be described, by way of example, with reference to the accompanying drawings, in which:

Fig. 1 is a cross section view of a first semiconductor substrate with an epitaxial layer of graded $Si_{1-x}Ge_x$ and a relaxed layer of $Si_{1-y}Ge_y$ covered with an encapsulation layer.

Fig. 2 is a cross section view of the first semiconductor substrate shown in Fig. 1 exposed to an ion bombardment of hydrogen resulting in a H-rich defective layer within the relaxed $Si_{1-y}Ge_y$ layer.

Fig. 3 is a cross section view of the first semiconductor substrate shown in Fig. 2 bonded to a second substrate with an insulator layer therein between.

Fig. 4 is a cross section view of separation at the H-rich defective layer within the relaxed $Si_{1-y}Ge_y$ layer during heat treatments, resulting in

transfer of a thin layer of relaxed $Si_{1-y}Ge_y$ or a plurality of layers containing the relaxed $Si_{1-y}Ge_y$ and the insulator layer from the first semiconductor substrate on to the second substrate shown in Fig. 3.

Fig. 5 is a cross section view of a first alternate embodiment of the invention having a smoothed surface of relaxed $Si_{1-y}Ge_y$ after Chemo-Mechanical Polishing (CMP).

Fig. 6 is a cross section view of a second alternate embodiment of the invention having a smoothed surface of relaxed $Si_{1-y}Ge_y$ after Chemo-Mechanical Polishing (CMP).

Fig. 7 is a cross section view of a thin layer of strained Si/SiGe grown on the upper surface of the embodiment shown in Fig. 5 with an optional thin layer of relaxed $Si_{1-y}Ge_y$ therein between.

Fig. 8 is a cross section view of a smoothed surface of the relaxed $Si_{1-y}Ge_y$ remaining on the first substrate after Chemo-Mechanical Polishing (CMP).

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

The drawings illustrate the steps for the production of a thin layer of monocrystalline strained Si or strained SiGe on SiGe on insulator (SGOI) substrates with the aid of planarization of surfaces, wafer bonding and H-induced layer separation and transfer techniques.

Referring now to Fig. 1, a cross section view of a partial embodiment of the invention is shown comprising a substrate 10 and a plurality of layers 20, 30 and 40. Substrate 10 may be a single crystal material such as Si, SiGe, SiGeC, SiC, GaAs, InP, etc. suitable for forming epitaxial layers thereon. An epitaxial graded layer 20 of $Si_{1-x}Ge_x$ is formed on the upper surface 12 of substrate 10. The upper surface 22 of graded layer 30 is substantially relaxed or completely relaxed. The relaxation may be due to a modified Frank-Read mechanism described by LeGoues et al. in U.S. Pat. No. 5,659,187 which issued on Aug. 19, 1997 and is incorporated herein by reference. Formation of graded SiGe layer 20 may be formed as described in U.S. Pat. No. 5,659,187 by LeGoues et al. Layer 20 as well as layer 30 (to be described below) may be formed in a

UHV CVD process as described in U.S. Pat. No. 5,298,452 by B.S. Meyerson which issued Mar. 29, 1994 and is incorporated herein by reference. In layer 20, the concentration x of Ge may range from zero to a value in the range from 0.2 to 0.5. Layer 20 may have a thickness in the range from about 3,000 angstroms to 1000 nm.

Epitaxial layer 30 is comprised substantially or completely of relaxed $Si_{1-y}Ge_y$ and is formed on upper surface 22 of layer 20. Layer 30 may have a thickness in the range from 200nm to 1000nm. The Ge content y in layer 30 is chosen to match the crystal lattice constant of upper surface 22 of layer 20 such that layer 30 is relaxed or essentially strain free. The Ge content y in layer 30 may be equal to or about the value of x at upper surface 22. The value y may be in the range from about 0.2 to about 0.5. An encapsulation layer 40 may be formed over relaxed layer 30. Encapsulation layer 40 may be deposited via PECVD, LPCVD, UHV CVD or spin-on techniques. The encapsulation material may be, for example, Si, SiO_2, Poly Si, Si_3N_4, low-k dielectric materials, for example, Diamond Like Carbon (DLC), Fluorinated Diamond Like Carbon (FDLC), a polymer of Si, C, O, and H or a combination of any two or more of the foregoing materials. One example of a polymer of Si, C, O, and H is SiCOH described in US Serial No. 09/107567 filed Jun. 29, 1998 by Grill et al. entitled "Hydrogenated Oxidized Silicon Carbon Material" (Docket YOR919980245US1) which is incorporated herein by reference. The deposition temperature for forming layer 40 may be below 900°C. The thickness of the encapsulation layer is in the range from about 5nm to about 500nm. Encapsulation layer 40 functions to protect upper surface 32 of layer 30 or to provide an isolation layer.

Fig. 2 shows substrate 10 from Fig. 1 with SiGe epitaxial layers 20 and 30 and an encapsulation layer 40. Layers 40 and 30 are subjected to ion bombardment for the implantation of hydrogen ions 50. Hydrogen ions 50 may be H^+ or H_2^+ and preferably H_2^+. H_2^+ may be implanted at an energy in the range from about 30 KeV to about 200 KeV at a dose in the range from $3x10^{16}$ to $1x10^{17}$ ions/cm^2. The hydrogen implantation results in the formation of a H-rich layer 70. Layer 70 comprises hydrogen-containing SiGe point defects and planar micro cracks residing in principle crystallographic planes of SiGe. The energy of hydrogen ions 50 is selected to place the peak dose in layer 30 below surface 32 in the range from 100 nm to 1000 nm below surface 32. The hydrogen-rich SiGe layer 70 will form at the peak dose location of hydrogen.

After the step of implanting hydrogen, a second substrate 80 is bonded to layer 40. Prior to wafer bonding, surface 42 of layer 40 is polished by a Chemo-Mechanical Polishing (CMP) process to smooth surface 42 to a planar surface having a root mean square (RMS) in the range from .3 nm to 1 nm. Surface 42 may be polished before or after the step of implantation of hydrogen ions 50. Substrate 80 may be a semiconductor such as Si, SiGe, SiGeC or SiC; an insulator such as sapphire, glass or ceramic; or a metal and has an upper surface 90 which may be polished as above to provide a smooth upper surface 90 having a RMS in the range from about 0.3 nm to about 1 nm. The surface roughness or RMS may be determined by performing measurements with an Atomic Force Microscope (AFM) over an area of 20 x 20 microns.

The top surface 42 of layer 40 shown in Fig. 2 is turned upside down and brought into contact with surface 90 of substrate 80. The two surfaces 42 and 90 are brought together by the wafer bonding approach. Surfaces 42 and 90 are bonded together initially without affecting the integrity of layer 70. Layer 70 shall remain intact mechanically while surfaces 42 and 90 are bonded together by annealing at a temperature in the range from about 20°C to about 500°C for a time period in the range from about 2 hours to about 50 hours.

Layer 30 is then separated at layer 70 by annealing at a temperature in the range from 200 °C to 600 °C without disturbing the mechanical bond between surface 42 of layer 40 and surface 90 of substrate 80. Layer 30 when separated at layer 70 forms a new upper surface 75 of relaxed $Si_{1-y}Ge_y$ layer 74 which is the upper portion of layer 30, structure 82, after separation shown in Fig. 4. Also surface 73 of relaxed $Si_{1-y}Ge_y$ layer 72 is formed which is the lower portion of layer 30, structure 81, shown in Fig. 4. Layer 74, layer 40 and substrate 80 form SGOI which is structure 82 shown in Fig. 4. The thickness or depth of layer 74 is controlled by the ion bombardment energy such that surface 75 of layer 74 is away from the interface of layers 30 and 20 and therefore contains much less dislocation defects. Surface 75 of $Si_{1-y}Ge_y$ layer 74 with encapsulation layer 40 below may have a surface roughness in the range from about 3 nm to about 15 nm root mean square (RMS). Surface 75 is then smoothed with a Chemo-Mechanical Polishing (CMP) process. The Chemo-Mechanical Polishing (CMP) process may also be needed to thin down the SiGe for some specific applications, e.g., the SiGe may be thinned to a thickness in the range of

about 30nm to about 200nm for VLSI applications. The surface roughness of surface 75 after CMP is in the range from about 0.3 to about 1 nm RMS.

An example of a smoothing process for surface 75 of $Si_{1-y}Ge_y$ layer 74 by Chemical Mechanical Polishing (CMP) includes a slurry, a 1 psi down force, a 50 rpm of table speed, a 30 to 60 rpm carrier speed and a 0.5 psi backside air pressure. The polishing slurry may be SC112 commercially available from Cabot Corporation, Aurora, Illinois. The slurry flow rate may be 140 milliliters/minute. The polishing slurry may have a pH from about 9.5 to about 11.0. The weight % of solids, which contains silica or may be only silica, may be in the range from about 5% to about 30% (a greater range than is in SC112) and the silica particle size may be in the range from about 12 to about 200 nanometers (a greater range than is in SC112). The CMP may be performed in a Westech 372 polishing tool, which comprises a circular rotating polishing platen and a rotating wafer carrier.

The polishing pad system may be a two pad stacked system. The top pad may be product No. IC1000 and the subpad may be product No. Suba IV; both pads are commercially available from Rodel Corporation, Newark, Delaware. The top pad may be initially conditioned such as using a fixed abrasive (such as diamond) for 300 seconds before polishing. The pad is then conditioned for 25 seconds before each wafer is smoothed.

After the CMP process step, a brush cleaning step is performed. The brush cleaning is effective in removing residual abrasive particles from the wafer surface left from CMP. The brush cleaning step was performed using a conventional double-sided roller brush cleaner containing one stage of brush cleaning. The time duration of the roller brush cleaning step was 99 seconds.

After removing 100-300 nm of surface 75 of $Si_{1-y}Ge_y$ layer 74, the roughness (RMS) of epitaxially grown $Si_{1-y}Ge_y$ layer, where y is 0.15 i.e. 15% Ge, was reduced from 5-6nm to 0.5-0.8nm in Root-Mean-Squre (RMS), which is acceptable or qualified for epitaxial growth. With surface 75 of layer 74 smoothed and in condition for epitaxial growth thereon, Si or SiGe may be grown thereon by UHV CVD. Depending on the composition of the grown SiGe and the existing SiGe of layer 74, strained Si or SiGe is formed due to lattice mismatch determined by the difference in compositions.

Smoothing or planarization of SiGe for epitaxial growth has been shown in U.S. 6,107,653 by E.A. Fitzgerald in an epitaxial growth application on bulk silicon. In U.S. 6,107,653, chemo-mechanical polishing (CMP) of the upper surface of a graded SiGe layer was performed to remove the roughness created by dislocations introduced during relaxation of the SiGe layer. The planarization of the surface was for the purpose of preventing the continued roughening and grooving of the surface that leads to dislocation blocking. Planarization prevented a rise in the threading dislocation density during subsequent growth of the graded SiGe layer.

For a further description of CMP of SiGe and other materials to reduce surface roughness to below 1 nm RMS, reference is made to Serial No. 09/_____ by D.F. Canaperi et al. filed on even date of Sept. 29, 2000 entitled "A Method of Wafer Smoothing for Bonding Using Chemo-Mechanical Polishing (CMP)" which is assigned to the assignee herein and incoroporated herein by reference.

For a description of forming strained Si/SiGe for high speed CMOS devices reference is made to U.S. Pat. No. 5,534,713 by Ismail et al. which issued on July 9, 1996, U.S. Serial No. 09/267323 by Chu et al. (Docket YOR9-1999-0460US1) filed Mar. 12, 1999 which is assigned to the assignee herein and incorporated herein by reference and PCT Application No. US00/06258 by J.O. Chu (Docket YOR9-1999-0123PCT1) having a priority date of March 12, 1999 which is assigned to the assignee herein and incorporated herein by reference.

In an alternate embodiment, structure 82' includes substrate 80 with an insulator layer 83 between substrate 80 and layer 40 which is shown in Fig. 5. The insulator layer 83 may be deposited or formed via PECVD, LPCVD, UHV CVD, thermal oxidation or spin-on techniques. Insulator layer 83 may comprise a material selected from the group consisting of SiO_2, Si_3N_4, Al_2O_3, or other acceptable or qualified low-k dielectric materials, for example, Diamond Like Carbon (DLC), Fluorinated Diamond Like Carbon (FDLC), a polymer of Si, C, O, and H such as SiCOH or a combination of any two or more of the foregoing materials. The deposition temperature is below 900°C.

Insulator layer 83 may have an upper surface 84 which is polished via CMP in place of or in addition to surface 90 and may be bonded to upper surface 42 of layer 40. If insulator layer 40 is not present over relaxed $Si_{1-y}Ge_y$ layer 30 which after separation is layer 74, insulator layer 83 may be bonded directly to upper surface 32 of layer 74. The bonding steps for bonding insulator layer 83 to insulator layer 40 include annealing at a temperature in the range from about 20°C to about 500°C and for a time period in the range from about 2 hours to about 50 hours. The bonding steps for bonding insulator layer 83 to relaxed $Si_{1-y}Ge_y$ layer 30 include annealing at a temperature in the range from about 20 °C to about 500 °C and for a time period in the range from about 2 hours to about 50 hours.

In another embodiment, structure 82'' includes intermediate layer 86 formed with or in place of insulator layer 83. Fig. 6 shows layer 86 in place of layer 83 shown in Fig. 5. Layer 86 has an upper surface 87 bonded to surface 42 of layer 40. Intermediate layer 86 may be Ge, or metals which either have a low-melting point or react with silicon to form a silicide such as tungsten (W) or cobalt (Co) to achieve high bonding strength at anneal temperatures in the range from about 100°C to about 800°C. The anneal can be either a furnace anneal or a rapid thermal anneal (RTA). Depending on the selection of intermediate layer 86, the bonding interface can be between SiGe layer 74 and Ge or a metal or between the encapsulation layer 40 and Ge or a metal.

Fig. 7 shows a cross section view of structure 82''' including structure 82 shown in Fig. 4 with epitaxial layers 94 and 98 formed on upper surface 75 of layer 74. Layer 94 may be a thin layer in the range from about 30nm to about 500nm of relaxed epitaxial $Si_{1-y}Ge_y$ and layer 98 may be a thin layer in the range from about 100 angstroms to about 300 angstroms of strained Si. Field effect transistors for CMOS or MODFET's may be formed in strained Si layer 98. The strain in Si will be tensile and the mobility of holes and electrons will be increased due to the tensile strain.

Fig. 8 shows a cross section view of structure 81' shown in Fig. 4 with upper surface 73' smoothed after Chemo-Mechanical Polishing (CMP) to provide a relaxed $Si_{1-y}Ge_y$ surface suitable for epitaxial deposition of additional $Si_{1-y}Ge_y$ to rebuild the thickness of layer 72' back to the thickness of original layer 30 shown in Fig. 1 or to another selected

thickness. An additional layer 40 may be formed over surface 73' of layer 72' (not shown) to provide the embodiment shown in Fig. 1 for starting another sequence of steps as shown in Figs. 2-4. Alternatively, the embodiment shown in Fig. 8 may be used for starting another sequence of steps as shown in Figs. 2-4.

It should be noted in the drawing that like elements or components are referred to by like and corresponding reference numerals.

While there has been described and illustrated a method for forming strained Si or SiGe on SiGe on insulator (SGOI) using planarization, cleaning, bonding and layer separation by the implantation of hydrogen, it will be apparent to those skilled in the art that modifications and variations are possible without deviating from the broad scope of the invention which shall be limited solely by the scope of the claims appended hereto.

CLAIMS

1. A method of preparing a relaxed SiGe layer on an insulator, comprising the steps of forming a graded $Si_{1-x}Ge_x$ epitaxial layer on a first single crystalline semiconductor substrate, forming a relaxed $Si_{1-y}Ge_y$ epitaxial layer over the graded $Si_{1-x}Ge_x$ layer, forming a hydrogen-rich defective layer in the relaxed $Si_{1-y}Ge_y$ layer by hydrogen bombardment, providing a layer of an insulator over the surface of the relaxed $Si_{1-y}Ge_y$ layer, and separating the relaxed $Si_{1-y}Ge_y$ layer at the hydrogen-rich defective layer to form a first structure containing the first substrate, the graded $Si_{1-x}Ge_x$ layer and a relaxed $Si_{1-y}Ge_y$ layer, and a second structure containing the insulator layer with a relaxed $Si_{1-y}Ge_y$ layer on its surface.

2. The method of claim 1, wherein the step of providing a layer of an insulator over the surface of the relaxed $Si_{1-y}Ge_y$ layer comprises selecting a second substrate having an insulator layer thereon, and bonding the surface of the relaxed $Si_{1-y}Ge_y$ epitaxial layer on the first substrate to the surface of the insulator layer on the second substrate, whereby the second structure contains the second substrate and the insulator layer with the relaxed $Si_{1-y}Ge_y$ layer on its surface.

3. The method of claim 1, wherein the step of providing a layer of an insulator over the surface of the relaxed $Si_{1-y}Ge_y$ layer comprises forming an insulator layer thereon, the method further comprising selecting a second substrate, and bonding the second substrate to the insulator layer, whereby the second structure contains the second substrate and the insulator layer with the relaxed $Si_{1-y}Ge_y$ layer on its surface.

4. The method of any preceding claim, further including the step of growing an epitaxial layer on the surface of the relaxed $Si_{1-y}Ge_y$ layer of the second structure.

5. The method of claim 4, wherein the epitaxial layer is a strained layer.

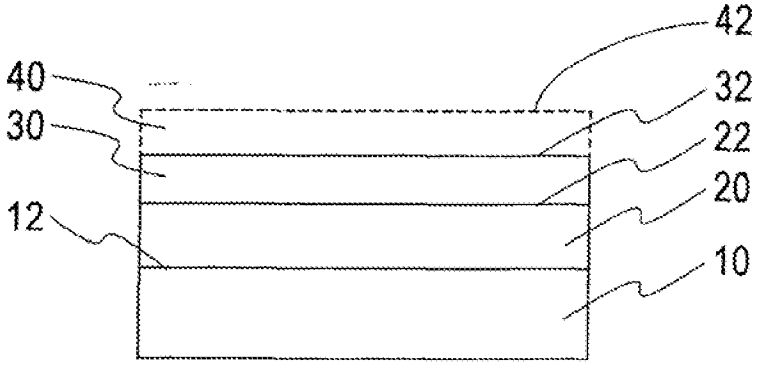

Fig. 1

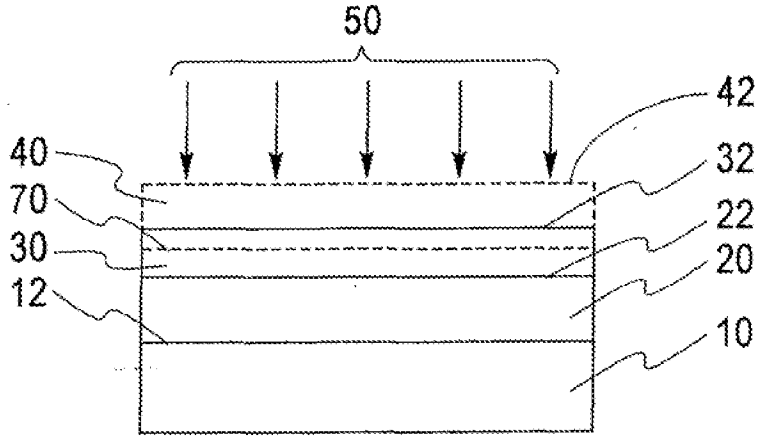

Fig. 2

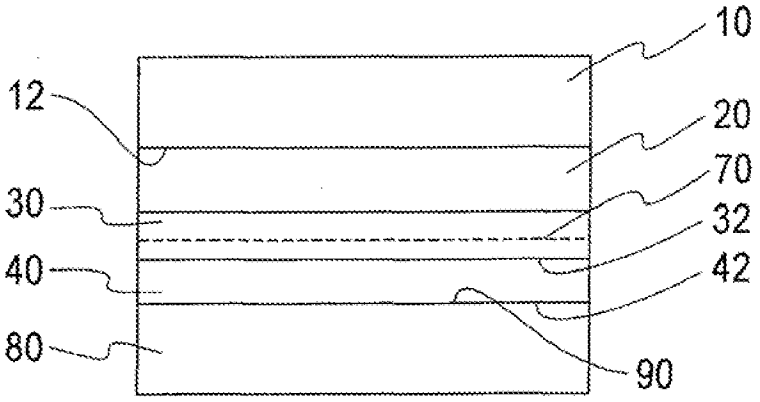

Fig. 3

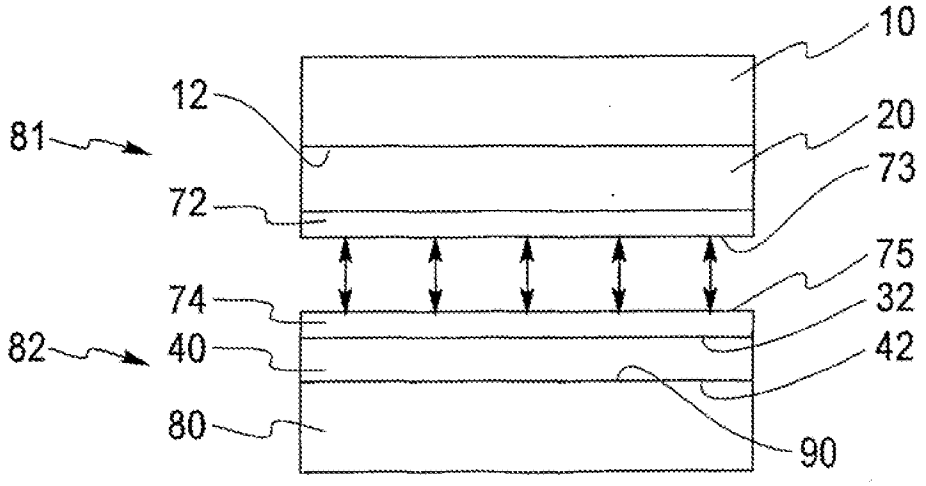

Fig. 4

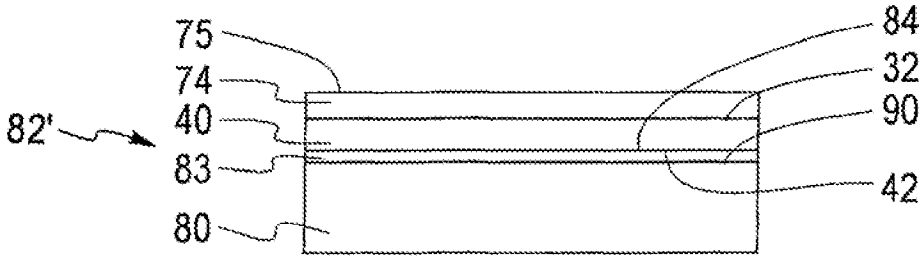

Fig. 5

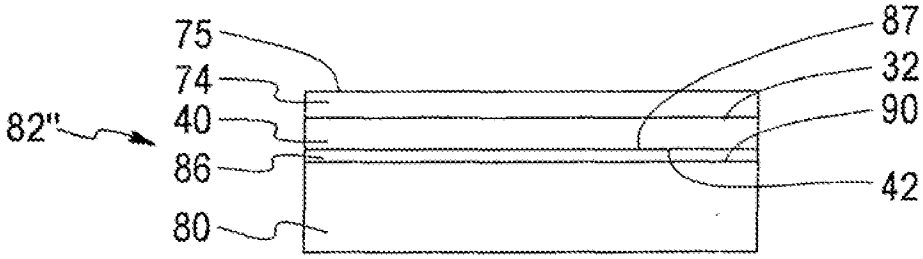

Fig. 6

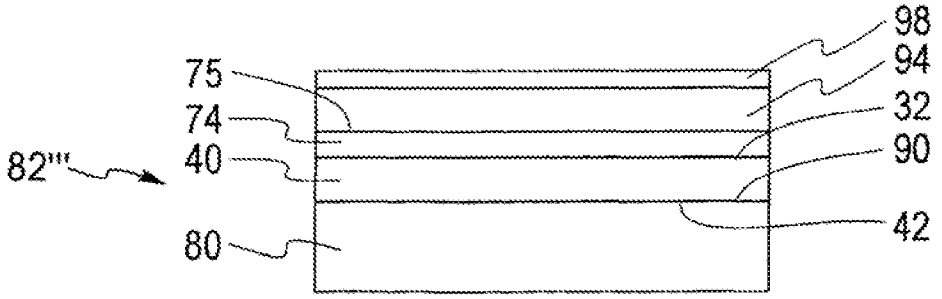

Fig. 7

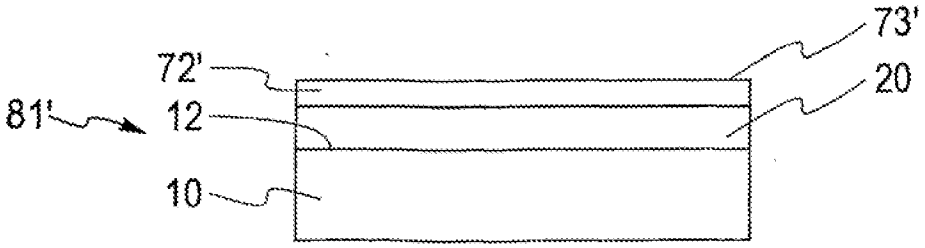

Fig. 8

INTERNATIONAL SEARCH REPORT

In International Application No
PCT/GB 01/04321

A. CLASSIFICATION OF SUBJECT MATTER
IPC 7 H01L21/762 H01L21/20

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC 7 H01L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)
EPO-Internal, WPI Data, PAJ, INSPEC

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	US 5 882 987 A (SRIKRISHNAN KRIS V) 16 March 1999 (1999-03-16) cited in the application column 4, line 8 -column 6, line 10; figures 4,5	1-3
A	MIZUNO T ET AL: "High performance strained-Si p-MOSFETs on SiGe-on-insulator substrates fabricated by SIMOX technology" ELECTRON DEVICES MEETING, 1999. IEDM TECHNICAL DIGEST. INTERNATIONAL WASHINGTON, DC, USA 5-8 DEC. 1999, PISCATAWAY, NJ, USA,IEEE, US, 5 December 1999 (1999-12-05), pages 934-936, XP010372110 ISBN: 0-7803-5410-9 cited in the application the whole document	1,4,5

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[X] Further documents are listed in the continuation of box C.

[X] Patent family members are listed in annex.

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"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art.

"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
8 February 2002	22/02/2002

Name and mailing address of the ISA	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL - 2280 HV Rijswijk Tel. (+31-70) 340-2040, Tx. 31 651 epo nl, Fax: (+31-70) 340-3016	Klopfenstein, P

INTERNATIONAL SEARCH REPORT

International Application No
PCT/GB 01/04321

C.(Continuation) DOCUMENTS CONSIDERED TO BE RELEVANT

Category °	Citation of document, with indication,where appropriate, of the relevant passages	Relevant to claim No.
P,A	HUANG L J ET AL: "SIGE-ON-INSULATOR PREPARED BY WAFER BONDING AND LAYER TRANSFER FOR HIGH-PERFORMANCE FIELD-EFFECT TRANSISTOR" APPLIED PHYSICS LETTERS, AMERICAN INSTITUTE OF PHYSICS. NEW YORK, US, vol. 78, no. 9, 26 February 2001 (2001-02-26), pages 1267-1269, XP001020601 ISSN: 0003-6951 page 1267; figure 1	1-5

INTERNATIONAL SEARCH REPORT

Information on patent family members

In nal Application No
PCT/GB 01/04321

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
US 5882987 A	16-03-1999	JP 3037934 B2	08-05-2000
		JP 11121377 A	30-04-1999